

RODIME RO 650 (A) SERIES DISK DRIVE

PRODUCT SPECIFICATION

PRO - 00126

REVISION 1

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1.0 INTRODUCTION

The RO 650 is a 3.5 inch 20 Megabyte Winchester disk drive which interfaces to any ANSI X3T9.2 SCSI (Small Computer System Interface) standard host interface.

The drive and controller electronics use VLSI and surface mounting techniques to allow integration within the standard 3.5 inch form factor.

2.0 SCOPE

This document describes the physical and functional characteristics of the RODIME RO 650 3.5 inch Winchester disk drives. It also specifies interface, programming, installation and environmental requirements.

3.0 RELATED DOCUMENTS

ANSI X3T9.2/82-2
COMMON COMMAND SET (CCS)

REV 17B
REV 4A

SCSI
FEBRUARY 28TH, 1986

Further detailed information referring to the use of the RO 650 series disk drives on a host system is given in the RO 650 User Manual.

4.0 PRODUCT DESCRIPTION

4.1 General

The RO 650 disk drive is a random access storage device which uses two 96mm magnetic disks to provide 20 Megabytes of formatted on-line storage.

The drive communicates with a host computer system via the Small Computer System Interface (SCSI) bus and is fully soft sectored.

4.2 Features

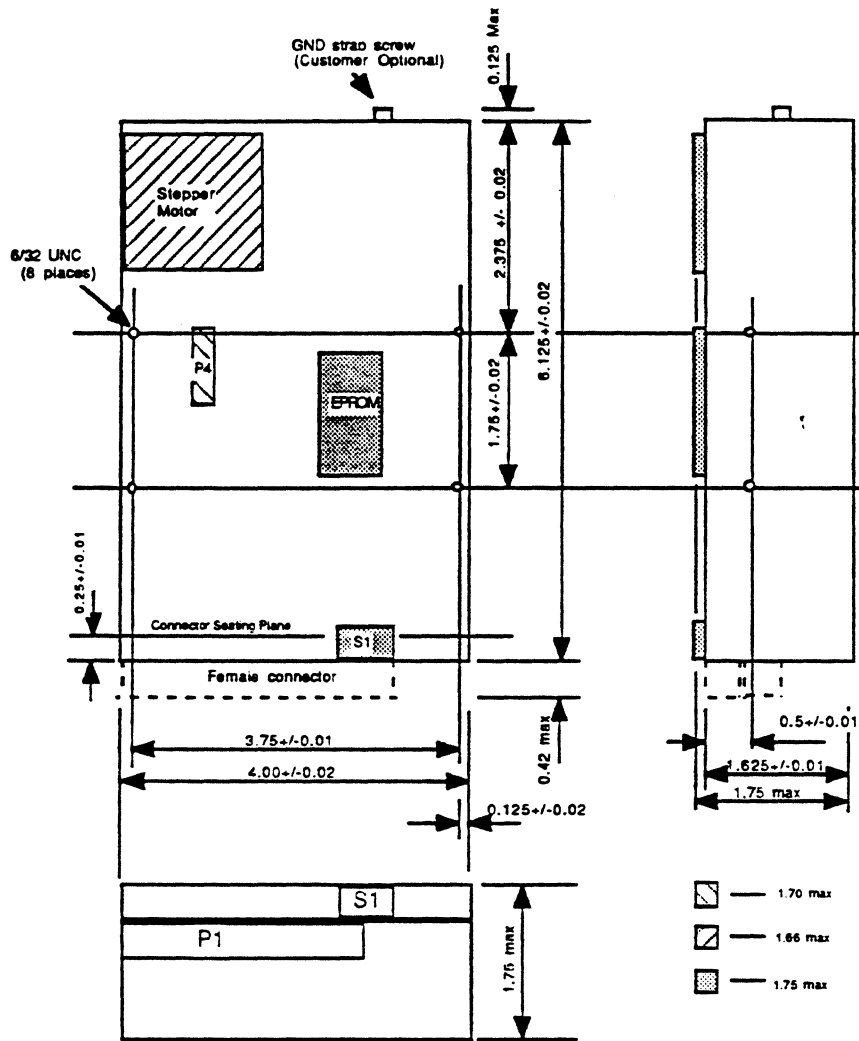
The RO 650 disk drive interface is compatible with the SCSI bus defined by ANSI X3T9.2/82-2 Revision 17B and Common Command Set (CCS) Revision 4A.

The following features are supported:

- a 4K bytes dual ported FIFO data buffer
- disconnected operations with arbitration for reselection
- command linking
- 32 bit ECC error detection and correction
- average data transfer rate of 937.5Kbytes/second
- 1 : 1 interleave factor with any format between 128 and 4096 bytes per sector.
- operation with arbitrating and non-arbitrating hosts
- extended SCSI command set
- diagnostics and error reporting.

4.3 Dimensions

The overall dimensions of the drive and mounting hole locations are shown in Figure 4.3.1.



All dimensions in inches

Female Connector : AMP 1-746094-0 (or similar)

FIGURE 4.3.1 RO 650A MOUNTING DETAILS

5.0 FUNCTIONAL DESCRIPTION

5.1 Recording Parameters

Data is recorded on both sides of the disks:

- 5.1.1 Flux density : 14,700 flux reversals per inch (max)
- 5.1.2 Bit density : 22,100 bits per inch (max)
- 5.1.3 Coding : (2,7) RLL
- 5.1.4 Track density : 600 tracks per inch (max)

5.2 Storage Capacity

- 5.2.1 Disks per drive : 2
- 5.2.2 Cylinders : 306
- 5.2.3 Tracks per cylinder : 4
- 5.2.4 Bytes per track : 20,484
- 5.2.5 Tracks per drive : 1,224
- 5.2.6 Capacity (Megabytes) : 25.50

5.3 Storage Capacity (Formatted)

- 532 byte sectors x 32 : 20.84 Megabytes
- 512 byte sectors x 33 : 20.68 Megabytes
- 256 byte sectors x 59 : 18.49 Megabytes

5.4 Rotational Parameters

- Disk rotational speed : 2746 $\pm$ 27 rpm

5.5 Cylinder Seek Time

The cylinder seek time includes settling time

5.5.1 Single cylinder : 18ms (average)

5.5.2 305 cylinders : 180ms (maximum)

5.5.3 Average cylinder seek : 85ms

In the above, average cylinder seek is defined as the total time for all possible cylinder seeks divided by the number of all possible cylinder seeks.

5.6 Illegal Addresses

There are no illegal addresses. The drive is shipped with all defects found during manufacture and test mapped to spare sectors. Refer to Section 14.0.

5.7 Power Interface

The RO 650 series drives require DC power only. The voltages are specified at connector J2 on the drive.

	<u>Current Typical</u> (Drive Selected) (Amperes)	<u>Current Maximum</u> (Drive Selected) (Amperes)
+5V DC ($\pm 5\%$)	0.95	1.20
+12V DC ($\pm 5\%$)	0.67	0.9

At power on the drive circuitry draws 2.5A max at +12V.

If the drive is not selected, the +12V current requirement is reduced by 0.25A (Typical).

5.7.1 The 12V must follow the 5V within 3 seconds if the 5V is applied first.

5.7.2 When checking the power supplies, the following loads should be used:

For the 12V supply, the power-up current may be measured using a standard load of 4.8 ohms and the operating current may be measured using 18 ohms. With a 1 ohm resistive load on the 5V supply and the above loads on the 12V supply, noise and ripple should not exceed 100mV peak to peak up to 500Hz and 50mV peak to peak from 500Hz to 25MHz.

5.7.3 In operation, the maximum rate of change of the 12V load due to the disk drive is 2A/ms.

5.7.4 Average power dissipation: 13.0 Watts (drive selected)

9.0 Watts (drive deselected)

If the drive is stopped using the START/STOP UNIT command (Section 13.14), the average power dissipation reduces to 7.0 Watts.

5.8 Data Transfer Rate

Average - 937.5 Kbytes/sec

5.9 Weight

1kg (2.2lb) maximum

6.0 RELIABILITY AND SERVICE GOALS

6.1 Drive Life

The minimum drive service life is 36,000 Power On Hours. The drive is capable of 10,000 start/stop operations during service life.

6.2 Mean Time Between Failure

The mean time between failure (MTBF) of any of the Rodime 650 drives shall exceed 12,000 hours where the first 50 hours of actual usage are excluded.

6.3 Service Goals

No preventative maintenance is required and there are no adjustments on the drive. The repairs that may be effected on-site are replacement of the electronics board. The mean time to repair (MTTR) including initial verification is 0.25 hours.

6.4 Data Reliability

The read error rates quoted below assume that the data has been verified as written correctly and all media defects flagged. Furthermore the drive must be operating within the specified operation environment.

6.4.1 Recoverable data error rate : 1 in 10^{10} bits read

6.4.2 Non-recoverable data error
rate across SCSI interface : 1 in 10^{12} bits read

NOTE

A recoverable error is a soft error which can be recovered with read retries.

A non-recoverable error is a hard error which cannot be recovered with 4 read retries. The non-recoverable error rate as specified excludes the effect of correction. The average correction time for 512 byte sector format is 95ms.

6.5 Actuator Reliability

A seek error occurs when the actuator moves to an incorrect cylinder. This occurrence shall not exceed 1 seek error in 5×10^6 seeks.

7.0 OPERATING ENVIRONMENT

7.1 Temperature and Humidity

Ambient Temperature range	:	10°C to 50°C
Relative Humidity range (No condensation)	:	10% RH to 85% RH
Maximum wet bulb temperature	:	26°C
Maximum rate of change of temperature	:	10°C per hour

7.2 Shock and Vibration

The drive shall meet its specified performance while subjected to the following shock and vibration conditions injected through the mounting frame in any of three mutually perpendicular axes. Vibrations are sinusoidal and shocks half-cycle sinusoidal waveforms.

7.2.1 Vibration

1.0g peak acceleration, 10 Hz to 500 Hz.

Note that the condition of paragraph 7.4 must also be met.

7.2.2 Shock

10.0g peak acceleration in X and Y axes, 7.5g peak acceleration in Z axis, duration less than 10ms, maximum frequency 2 per second.

7.3 Radio Frequency Interference

Electric field shall not exceed 5 volt/meter r.m.s. in the range 1.5Hz to 500MHz.

7.4 Magnetic Field

There shall be no source of constant magnetic field which yields more than 0.0005 Tesla measured in the location occupied by the magnetic heads when the drive is installed.

7.5 Altitude

Altitude relative to sea level : +10,000 feet, -1,000 feet

7.6 Emitted Acoustic Noise

Peak emitted noise : 54 dBA (continuous, maximum)
at 1 metre from the nearest point on the drive.

8.0 NON-OPERATING ENVIRONMENT

8.1 Temperature and Humidity

Ambient Temperature range	:	-40°C to +70°C
Relative humidity range (no condensation)	:	5% RH to 90% RH
Maximum wet bulb temperature	:	30°C
Maximum rate of change of temperature	:	less than that which causes condensation

8.2 Shock and Vibration

8.2.1 Packed

The approved Rodime shipping container will protect the drive against damage when the container is subjected to the following shipping shock and vibration:

- (a) Vibration : 0.2 inches peak to peak displacement, 5Hz to 20Hz;
: 3.5g peak acceleration, 20Hz to 500Hz.
- (b) Shock : Dropped to ground on any side or corner from 1 metre.

8.2.2 Unpacked

- (a) Vibration : 2.0g peak acceleration, 10Hz to 500Hz.
- (b) Shock : 40g peak acceleration in 2 axes parallel to PCB, 30g peak acceleration in axis perpendicular to PCB. Duration less than 10ms, maximum frequency 1 per 10 seconds.

9.0 HARDWARE INTERFACE

9.1 Drive Mounting and Installation

The RO 650 drive may be mounted in a host system in any orientation.

When installing the drive into an enclosure, the breather holes on the drive top cover must not be obstructed. At least 0.1 inch clearance must be provided between the top cover and the host frame.

There must be at least 0.1 inch clearance between the drive housing and the host frame to ensure functional vibration isolation.

The drive may be mounted in either a vertical or horizontal orientation. It is supplied complete with antivibration mounts and threaded mounting brackets.
See Figure 4.3.1.

10.0 PHYSICAL INTERFACE

This section contains the physical definition of the drive interface. The connectors, and bus timing needed to implement SCSI are covered.

10.1 Physical Description

SCSI devices are daisy-chained together using a common cable. Both ends of the cable are terminated. All signals are common between all SCSI devices.

The RO 650 uses single-ended drivers and receivers, which allow a maximum cable length of six metres.

10.2 Cable Requirements

A 50-conductor flat cable or 25-signal twisted-pair cable shall be used. The maximum cable length shall be 6.0 metres (19.7 ft).

A stub length of no more than 0.1 metres (3.94 in) is allowed off the mainline interconnection within any connected equipment.

A minimum conductor size of 28 AWG shall be employed to minimize noise effects and ensure proper distribution of optional terminator power.

10.3 Connector Requirements

The drive connector is a 50-conductor connector consisting of two rows of 25 male pins with adjacent pins 2.54 mm (0.1 in) apart.

The cable connector shall be a 50-conductor connector consisting of two rows of 25 female contacts with adjacent contacts 2.54mm (0.1 in) apart. The 3M P/N 3425-3000 cable connector is recommended.

The connector pin assignments are as shown in Table 10.3.1, and connector layout is shown in Figure 10.3.2.

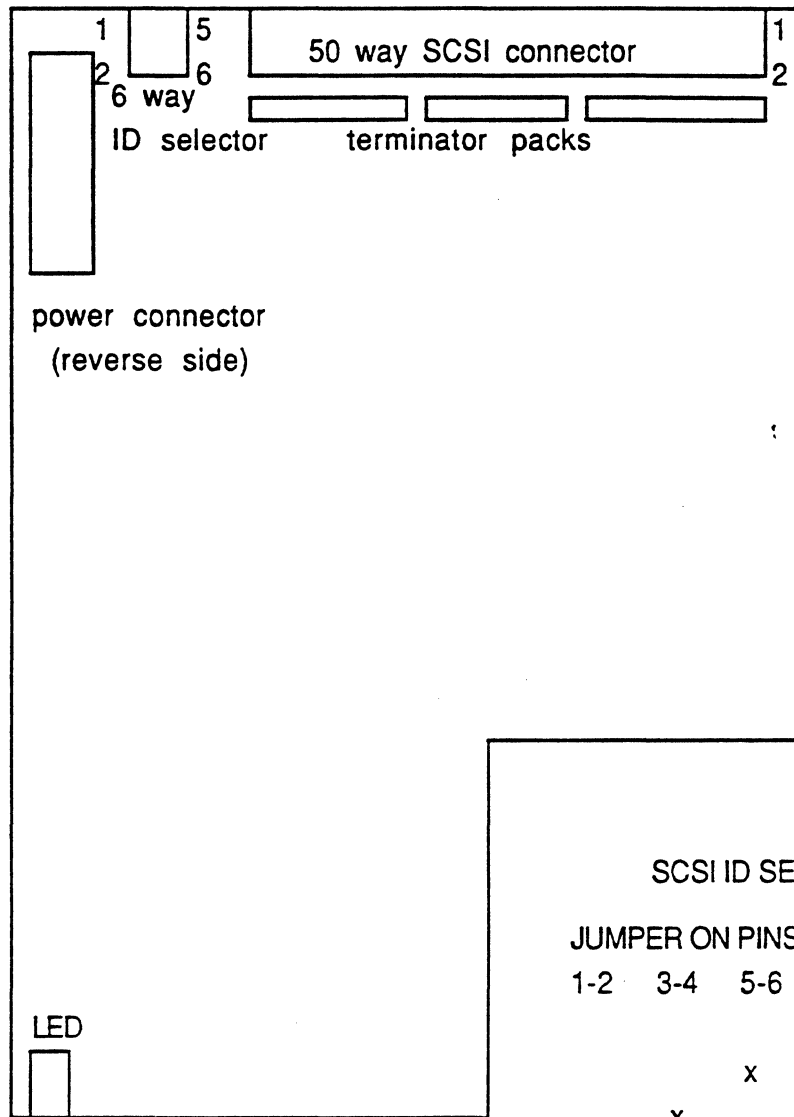
The power connector is a 4 pin AMP Mate-N-Lok P/N 350211-1 mounted on the reverse side of the PCB. See Figure 10.3.2. The recommended mating connector is AMP P/N 1-480424-0 socket housing using AMP pin P/N 350078-4.

TABLE 10.3.1 : PIN ASSIGNMENTS

<u>SIGNAL</u>	<u>PIN NUMBER</u>
-DB(0)	2
-DB(1)	4
-DB(2)	6
-DB(3)	8
-DB(4)	10
-DB(5)	12
-DB(6)	14
-DB(7)	16
-DB(P)	18
GROUND	20
GROUND	22
GROUND	24
TERMPWR	26
GROUND	28
GROUND	30
-ATN	32
GROUND	34
-BSY	36
-ACK	38
-RST	40
-MSG	42
-SEL	44
-C/D	46
-REQ	48
-I/O	50

NOTES:

- (1) All odd pins except pin 25 shall be connected to ground. Pin 25 should be left open.
- (2) The minus sign next to the signals indicates active low.



SCSI ID SELECTION			DRIVE ID
JUMPER ON PINS	1-2	3-4	
			0
		x	1
	x		2
	x	x	3
x			4
x		x	5
x	x		6
x	x	x	7

FIGURE 10.3.2 : RO 650 CONNECTOR LAYOUT

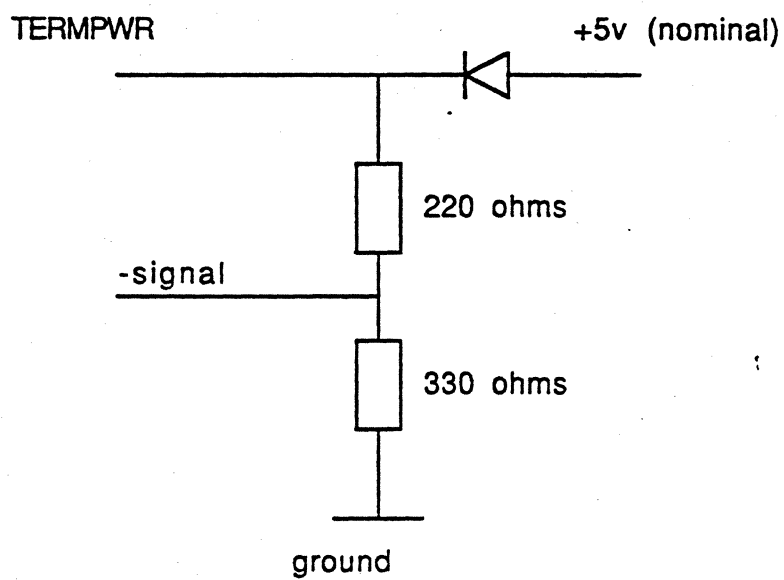


FIGURE 10.4.1 : RO 650 TERMPWR CONNECTION

10.4 Electrical Description

All assigned signals are terminated with 220 ohms to +5v (nominal) and 330 ohms to ground at each end of the cable (See Figure 10.4.1). All signals use open-collector drives.

10.4.1 Output Characteristics

Each signal driven by the RO 650 has the following output characteristics when measured at the drive's connector:

Signal assertion = 0.0 volts dc to 0.4 volts dc.

Minimum driver output capacity = 48 milliamps (sinking) at 0.5 volts dc.

Signal negation = 2.5 volts dc to 5.25 volts dc.

10.4.2 Input Characteristics

Each signal received by the RO 650 shall have the following input characteristics when measured at the drive's connector:

Signal true = 0.0 volts dc to 0.8 volts dc.

Maximum total input load = -0.4 milliamp at 0.4 volts dc.

Signal false = 2.0 volts dc to 5.25 volts dc.

Minimum input hysteresis = 0.2 volts dc.

10.4.3 Terminator Power (Optional)

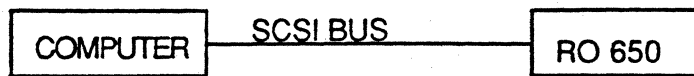
The RO 650 is configured to supply terminator power, (TERMPWR), with the following characteristics:

V_{term} = 4.0 volts dc to 5.25 volts dc.

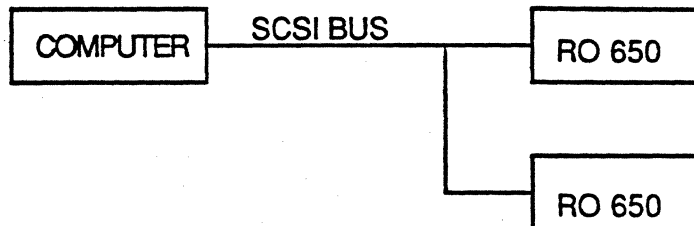
800 milliamps minimum source drive capability.

1.0 milliamp maximum sink capability.

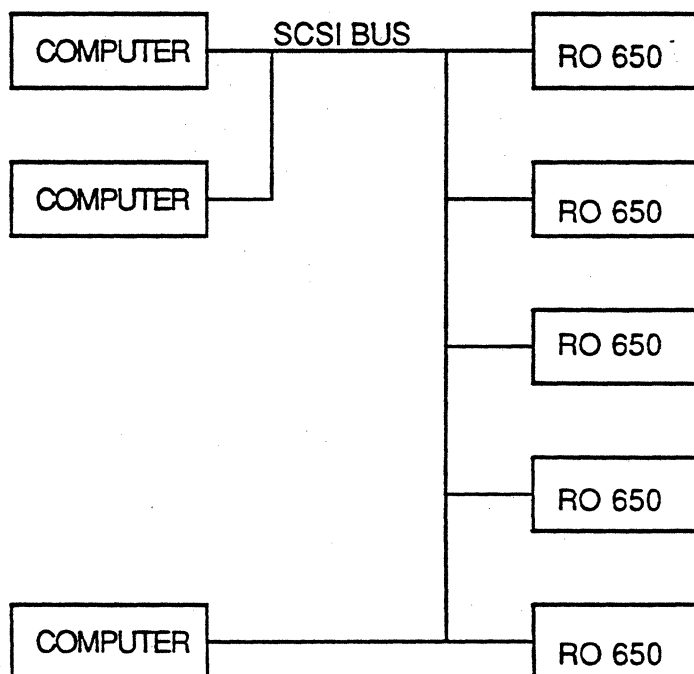
Figure 10.4.1 shows the RO 650 TERMPWR connection.



SINGLE INITIATOR, SINGLE TARGET



SINGLE INITIATOR, MULTIPLE TARGET



MULTIPLE INITIATOR, MULTIPLE TARGET

FIGURE 10.5.2 : SAMPLE SCSI CONFIGURATIONS

10.5 SCSI Bus

Communication on the SCSI bus is allowed between only two SCSI devices at any given time. There is a maximum of eight SCSI devices. Each SCSI device has an SCSI ID bit assigned as shown in Figure 10.5.1. The RO 650 assignment is shown in Figure 10.3.2.

When two SCSI devices communicate on the SCSI bus, one acts as an initiator and the other acts as a target. The initiator originates an operation and the target performs the operation. An SCSI device usually has a fixed role as an initiator or target.

Three sample system configurations are shown in Figure 10.5.2.

Up to eight SCSI devices can be supported on the SCSI bus. They can be any combination of initiators and targets.

Certain SCSI bus functions are assigned to the initiator and certain SCSI bus functions are assigned to the target. The initiator may arbitrate for the SCSI bus and select a particular target. The target may request the transfer of COMMAND, DATA, STATUS, or other information on the DATA BUS, and in some cases it may arbitrate for the SCSI bus and reselect an initiator for the purpose of continuing an operation.

Information transfers on the DATA BUS are asynchronous and follow a defined REQ/ACK handshake protocol. One byte of information may be transferred with each handshake.

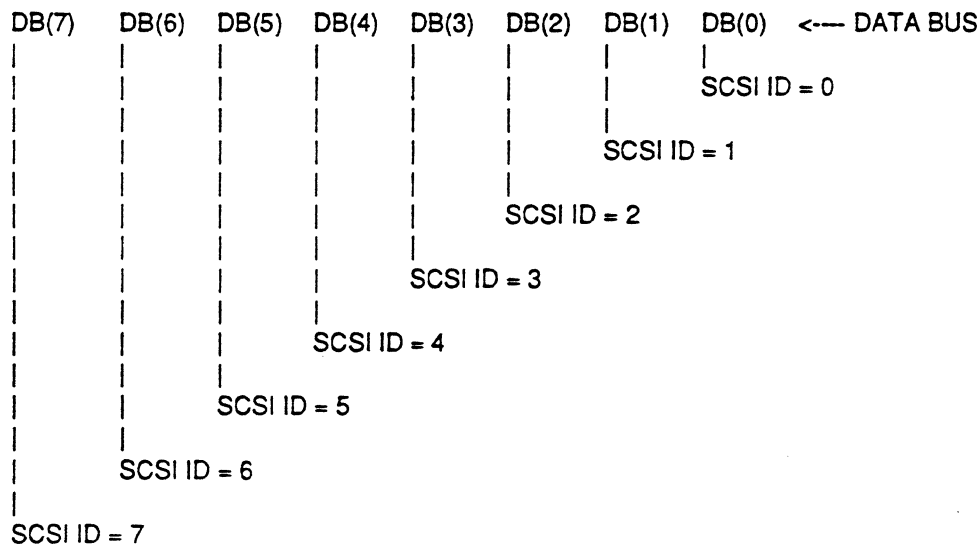


FIGURE 10.5.1 : SCSI ID BITS

10.6 SCSI Bus Signals

There are a total of eighteen signals. Nine are used for control and nine are used for data. (Data signals include the parity signal option). These signals are described as follows:

BSY (BUSY)

An "OR-tied" signal that indicates that the bus is being used.

SEL (SELECT)

A signal used by an initiator to select a target or by a target to reselect an initiator.

C/D (CONTROL/DATA)

A signal driven by a target that indicates whether CONTROL or DATA information is on the DATA BUS. True indicates CONTROL.

I/O (INPUT/OUTPUT)

A signal driven by a target that controls the direction of data movement on the DATA BUS with respect to an initiator. True indicates input to the initiator. This signal is also used to distinguish between SELECTION and RESELECTION phases.

MSG (MESSAGE)

A signal driven by a target during the MESSAGE phase.

REQ (REQUEST)

A signal driven by a target to indicate a request for a REQ/ACK data transfer handshake.

ACK (ACKNOWLEDGE)

A signal driven by an initiator to indicate an acknowledgement for a REQ/ACK data transfer handshake.

ATN (ATTENTION)

A signal driven by an initiator to indicate the ATTENTION condition.

RST (RESET)

An "OR-tied" signal that indicates the RESET condition.

DB(7-0,P) (DATA BUS)

Eight data-bit signals, plus a parity-bit signal that form a DATA BUS. DB(7) is the most significant bit and has the highest priority during the ARBITRATION phase. Bit number, significance, and priority decrease downward to DB(0). A data bit is defined as one when the signal value is true and is defined as zero when the signal value is false.

Data parity DB(P) is odd. The use of parity is a system option (ie a system is configured so that all SCSI devices on a bus generate parity and have parity detection enabled, or all SCSI devices have parity detection disabled or not implemented). Parity is not valid during the ARBITRATION phase.

10.6.1 Signal Values

Signals may assume true or false values. There are two methods of driving these signals. In both cases, the signal shall be actively driven true, or asserted. In the case of OR-tied drivers, the driver does not drive the signal to the false state, rather the bias circuitry of the bus terminators pulls the signal false whenever it is released by the drivers at every SCSI device. If any driver is asserted, then the signal is true. In the case of non-OR-tied drivers, the signal may be actively driven false, or negated. In this standard, wherever the term negated is used, it means that the signal may be actively driven false, or may be simply released (in which case the bias circuitry pulls it false), at the option of the implementor. The advantage to actively drive signals false is that the transition from true to false occurs more quickly, and noise margins may be somewhat improved; this may permit somewhat faster data transfer.

10.6.2 OR-Tied Signals

The BSY and RST signals shall be OR-tied only. In the ordinary operation of the bus, these signals are simultaneously driven true by several drivers. No signals other than BSY, RST, and DB(P) are simultaneously driven by two or more drivers, and any signal other than BSY and RST may employ OR-tied or non-OR-tied drivers. DB(P) shall not be driven false during the ARBITRATION phase. There is no operational problem in mixing OR-tied and non-OR-tied drivers on signals other than BSY and RST.

10.6.3 Signal Sources

Table 10.6.1 indicates which type of SCSI device is allowed to source each signal. No attempt is made to show if the source is driving asserted, driving negated, or is passive. All SCSI device drivers that are not active sources shall be in the passive state. Note that the RST signal may be sourced by any SCSI device at any time.

TABLE 10.6.1 : SIGNAL SOURCES

Bus Phase	Signals				
	BSY	SEL	C/D, I/O, MSG, REQ	ACK/ATN	DB(7-0,P)
BUS FREE	None	None	None	None	None
ARBITRATION	All	Winner	None	None	SCSI ID
SELECTION	I & T	Initiator	None	Initiator	Initiator
RESELECTION	I & T	Target	Target	Initiator	Target
COMMAND	Target	None	Target	Initiator	Initiator
DATA IN	Target	None	Target	Initiator	Target
DATA OUT	Target	None	Target	Initiator	Initiator
STATUS	Target	None	Target	Initiator	Target
MESSAGE IN	Target	None	Target	Initiator	Target
MESSAGE OUT	Target	None	Target	Initiator	Initiator

See key on page 21.

All: The signal shall be driven by all SCSI devices that are actively arbitrating.

SCSI ID: A unique data bit (the SCSI ID) shall be driven by each SCSI device that is actively arbitrating; the other seven data bits shall be released (ie not driven) by this SCSI device. The parity bit (DB(P)) may be undriven or driven to the true state, but shall never be driven to the false state during this phase.

I & T: The signal shall be driven by the initiator, target, or both, as specified in the SELECTION phase and RESELECTION phase.

Initiator: If this signal is driven, it shall be driven only by the active initiator.

None: The signal shall be released; that is, not be driven by any SCSI device. The bias circuitry of the bus terminators pulls the signal to the false state.

Winner: The signal shall be driven by the one SCSI device that wins arbitration.

Target: If the signal is driven, it shall be driven only by the active target.

10.7 SCSI Bus Timing

Unless otherwise indicated, the delay-time measurements for each SCSI device, shown in 10.7.1 through 10.7.14, shall be calculated from signal conditions existing at that SCSI device's own SCSI bus connection. Thus, these measurements (except cable skew delay) can be made without considering delays in the cable.

10.7.1 Arbitration Delay (2.2 microseconds)

The minimum time an SCSI device shall wait from asserting BSY for arbitration until the DATA BUS can be examined to see if arbitration has been won. There is no maximum time.

10.7.2 Assertion Period (90 nanoseconds)

The minimum time that a target shall assert REQ while using synchronous data transfers. Also, the minimum time that an initiator shall assert ACK while using synchronous data transfers.

10.7.3 Bus Clear Delay (800 nanoseconds)

The maximum time for an SCSI device to stop driving all bus signals after:

- (1) The BUS FREE phase is detected (BSY and SEL both false for a bus settle delay)
- (2) SEL is received from another SCSI device during the ARBITRATION phase
- (3) The transition of RST to true.

NOTE: For the first condition above, the maximum time for an SCSI device to clear the bus is 1200 nanoseconds from BSY and SEL first becoming both false. If an SCSI device requires more than a bus settle delay to detect BUS FREE phase, it shall clear the bus within a bus clear delay minus the excess time.

10.7.4 Bus Free Delay (800 nanoseconds)

The minimum time that an SCSI device shall wait from its detection of the BUS FREE phase (BSY and SEL both false for a bus settle delay) until its assertion of BSY when going to the ARBITRATION phase.

10.7.5 Bus Set Delay (1.8 microseconds)

The maximum time for an SCSI device to assert BSY and its SCSI ID bit on the DATA BUS after it detects BUS FREE phase (BSY and SEL both false for a bus settle delay) for the purpose of entering the ARBITRATION phase.

10.7.6 Bus Settle Delay (400 nanoseconds)

The time to wait for the bus to settle after changing certain control signals as called out in the protocol definitions.

10.7.7 Cable Skew Delay (10 nanoseconds)

The maximum difference in propagation time allowed between any two SCSI bus signals when measured between any two SCSI devices.

10.7.8 Data Release Delay (400 nanoseconds)

The maximum time for an initiator to release the DATA BUS signals following the transition of the I/D signal from false to true.

10.7.9 Deskew Delay (45 nanoseconds)

The minimum time required for deskew of certain signals.

10.7.10 Hold Time (45 nanoseconds)

The minimum time added between the assertion of REQ or ACK and the changing of the data lines to provide hold time in the initiator or target, respectively, while using synchronous data transfers.

10.7.11 Negation Period (90 nanoseconds)

The minimum time that a target shall negate REQ while using synchronous data transfers. Also, the minimum time that an initiator shall negate ACK while using synchronous data transfers.

10.7.12 Reset Hold Time (25 microseconds)

The minimum time for which RST is asserted. There is no maximum time.

10.7.13 Selection Abort Time (200 microseconds)

The maximum time that a target (or initiator) shall take from its most recent detection of being selected (or reselected) until asserting a BSY response. This timeout is required to ensure that a target (or initiator) does not assert BSY after a SELECTION (or RESELECTION) phase has been aborted.

10.7.14 Selection Timeout Delay (250 milliseconds, recommended)

The minimum time that an initiator (or target) should wait for a BSY response during the SELECTION (or DESELECTION) phase before starting the timeout procedure. Note that this is only a recommended time period. The specifications for the peripheral devices shall be consulted for the actual timing requirements.

11.0 LOGICAL CHARACTERISTICS

11.1 SCSI Bus Phases

The SCSI architecture includes eight phases:

BUS FREE phase

ARBITRATION phase

SELECTION phase

RESELECTION phase

COMMAND phase \

DATA phase \ These phases are collectively termed the information

STATUS phase / transfer phases.

MESSAGE phase /

The SCSI bus can never be more than one phase at any given time. Unless otherwise noted in the following descriptions, signals that are not mentioned shall not be asserted.

11.1.1 BUS FREE Phase

The BUS FREE phase is used to indicate that no SCSI device is actively using the SCSI bus and that it is available for subsequent users.

SCSI devices shall detect the BUS FREE phase after SEL and BSY are both false for at least a bus settle delay.

SCSI devices shall release all SCSI bus signals within a bus clear delay after BSY and SEL become continuously false for a bus settle delay. If an SCSI device requires more than a bus settle delay to detect the BUS FREE phase then it shall release all SCSI bus signals within a bus clear delay minus the excess time to detect the BUS FREE phase. The total time to clear the SCSI bus shall not exceed a bus settle delay plus a bus clear delay.

11.1.2 ARBITRATION Phase

The ARBITRATION phase allows one SCSI device to gain control of the SCSI bus so that it can assume the role of an initiator or target.

The procedure for an SCSI device to obtain control of the SCSI bus is as follows:

- (1) The SCSI device shall first wait for the BUS FREE phase to occur. The BUS FREE phase is detected whenever both BSY and SEL are simultaneously and continuously false for a minimum of a bus settle delay.
- (2) The SCSI device shall wait a minimum of a bus free delay after detection of the BUS FREE phase (ie after BSY and SEL are both false for a bus settle delay) before driving any signal.
- (3) Following the bus free delay in Step (2), the SCSI device may arbitrate for the SCSI bus by asserting both BSY and its own SCSI ID, however the SCSI device shall not arbitrate (ie assert BSY and its SCSI ID) if more than a bus set delay has passed since the BUS FREE phase was last observed.
- (4) After waiting at least an arbitration delay (measured from its assertion of BSY) the SCSI device shall examine the DATA BUS. If a higher priority SCSI ID bit is true on the DATA BUS (DB(7) is the highest), then the SCSI device has lost the arbitration and the SCSI device may release its signals and return to Step (1). If no higher priority SCSI ID bit is true on the DATA BUS, then the SCSI device has won the arbitration and it shall assert SEL. Any other SCSI device that is participating in the ARBITRATION phase has lost the arbitration and shall release BSY and its SCSI ID bit within a bus clear delay after SEL becomes true. An SCSI that loses arbitration may return to Step (1).
- (5) The SCSI device that wins arbitration shall wait at least a bus clear delay plus a bus settle delay after asserting SEL before changing any signals.

NOTE: The SCSI ID bit is a single bit on the DATA BUS that corresponds to the SCSI device's unique SCSI address. All other seven DATA BUS bits shall be released by the SCSI device. Parity is not valid during the ARBITRATION phase. During the phase, DB(P) may be undriven or driven to the true state, but shall not be driven to the false state.

11.1.3 SELECTION Phase

The SELECTION phase allows an initiator to select a target for the purpose of initiating some target function (eg READ or WRITE command).

NOTE: During the SELECTION phase the I/O signal shall be negated so that this phase can be distinguished from the RESELECTION phase.

11.1.3.1 Nonarbitrating Systems

In systems with the ARBITRATION phase not implemented, the initiator shall first detect the BUS FREE phase and then wait a minimum of a bus clear delay. Then, except in certain single initiator environments with initiators employing the single initiator option (see 11.1.3.4), the initiator shall assert the desired target's SCSI ID and its own initiator SCSI ID on the DATA BUS. After two deskew delays the initiator shall assert SEL.

11.1.3.2 Arbitrating Systems

In systems with ARBITRATION phase implements, the SCSI device that won the arbitration has both BSY and SEL asserted and has delayed at least a bus clear delay plus a bus settle delay before ending the ARBITRATION phase. The SCSI device that won the arbitration becomes an initiator by releasing I/O. Except in certain single initiator environments with initiators employing the single initiator option (see 11.1.3.4), the initiator shall set the DATA BUS to a value which is the OR of its SCSI ID bit and the target's SCSI ID bit. The initiator shall then wait at least two deskew delays and release BSY. The initiator shall then wait at least a bus settle delay before looking for a response from the target.

11.1.3.3 All Systems

In all systems, the target shall determine that it is selected when SEL and its SCSI ID bit are true and BSY and I/O are false for at least a bus settle delay. The selected target may examine the DATA BUS in order to determine the SCSI ID of the selecting initiator unless the initiator employed the single initiator option (see 11.1.3.4). The selected target shall then assert BSY within a selection abort time of its most recent detection of being selected; this is required for correct operation of the timeout procedure. In systems with parity implemented, the target shall not respond to a selection if bad parity is detected. Also, if more than two SCSI ID bits are on the DATA BUS, the target shall not respond to selection.

At least two deskew delays after the initiator detects BSY is true, it shall release SEL and may change the DATA BUS.

11.1.3.4 Single Initiator Option

Initiators that do not implement the RESELECTION phase and do not operate in the multiple initiator environment are allowed to set only the target's SCSI ID bit during the SELECTION phase. This makes it impossible for the target to determine the initiator's SCSI ID.

11.1.3.5 Selection Timeout Procedure

Two optional selection timeout procedures are specified for clearing the SCSI bus if the initiator waits a minimum of a selection timeout delay and there has been no BSY response from the target.

- (1) Optionally, the initiator shall assert the RST signal (see 11.2.2).
- (2) Optionally, the initiator shall continue asserting SEL and shall release the DATA BUS. If the initiator has not detected BSY to be true after at least a selection abort time plus two deskew delays, the initiator shall release SEL allowing the SCSI bus to go to the BUS FREE phase. SCSI devices shall ensure that when responding to selection that the selection was still valid within a selection abort time of their assertion of BSY. Failure to comply with this requirement could result in an improper selection (two targets connected to the same initiator, wrong target connected to an initiator, or a target connected to no initiator).

11.1.4 RESELECTION Phase

RESELECTION is an optional phase that allows a target to reconnect to an initiator for the purpose of continuing some operation that was previously started by the initiator but was suspended by the target, (ie the target disconnected by allowing a BUS FREE phase to occur before the operation was complete).

RESELECTION can only be used in systems that have ARBITRATION phase implemented.

Upon completing the ARBITRATION phase, the winning SCSI device has both BSY and SEL asserted and has delayed at least a bus clear delay plus a bus settle delay. The winning SCSI device becomes a target by asserting the I/O signal. The winning SCSI device shall also set the DATA BUS to a value that is the OR of its SCSI ID bit and the initiator's SCSI ID bit. The target shall wait at least two deskew delays and release BSY. The target shall then wait at least a bus settle delay before looking for a response from the initiator.

The initiator shall determine that it is reselected when SEL, I/O, and its SCSI ID bit are true and BSY is false for at least a bus settle delay. The reselected initiator may examine the DATA BUS in order to determine the SCSI ID of the reselecting target. The reselected initiator shall then assert BSY within a selection abort time of its most recent detection of being reselected; this is required for correct operation of the timeout procedure. In systems with parity implemented, the initiator shall not respond to a RESELECTION if bad parity is detected. Also, the initiator shall not respond to a RESELECTION if more than two SCSI ID bits are on the DATA BUS.

After the target detects BSY, it shall also assert BSY and wait at least two deskew delays and then release SEL. The target may then change the I/O signal and the DATA BUS. After the reselected initiator detects SEL false, it shall release BSY. The target shall continue asserting BSY until the target is ready to relinquish the SCSI bus.

11.1.4.1 RESELECTION Timeout Procedure

If the target waits a minimum of a selection timeout period and there has been no BSY response from the initiator, then the target shall clear the SCSI bus using the following procedure and continue attempts to reselect the initiator, clearing the bus between each attempt.

The target shall continue asserting SEL and I/O and shall release all DATA BUS signals. If the target has not detected BSY to be true after at least a selection abort time plus two deskew delays, the target shall release SEL and I/O allowing the SCSI bus to go to the BUS FREE phase.

11.1.5 Information Transfer Phases

The COMMAND, DATA, STATUS, and MESSAGE phases all grouped together as the information transfer phases because they are all used to transfer data or control information via the DATA BUS.

The C/D, I/O, and MSG signals are used to distinguish between the different information transfer phases (see Table 11.1.5). The target drives these three signals and therefore controls all the changes from one phase to another. The initiator can request a MESSAGE OUT phase by asserting ATN, while the target can cause the BUS FREE phase by releasing MSG, C/D, I/O, and BSY.

TABLE 11.1.5 : INFORMATION TRANSFER PHASES

Signal						
MSG	C/D	I/O	Phase Name	Direction of Transfer		Comment
0	0	0	DATA OUT	Initiator to target	\	Data
0	0	1	DATA IN	Initiator from target	/	Phase
0	1	0	COMMAND	Initiator to target		
0	1	1	STATUS	Initiator from target		
1	0	0	*			
1	0	1	*			
1	1	0	MESSAGE OUT	Initiator to target	\	Message
1	1	1	MESSAGE IN	Initiator from target	/	Phase

KEY: 0 = False
 1 = True
 * = Reserved for future standardization

The information transfer phases use one or more REQ/ACK handshakes to control the information transfer. Each REQ/ACK handshake allows the transfer of one byte of information. During the information transfer phases BSY shall remain true and SEL shall remain false. Additionally, during the information transfer phases, the target shall continuously envelope the REQ/ACK handshake(s) with C/D, I/O, and MSG in such a manner that these control signals are valid for a bus settle delay before the assertion of REQ of the first handshake and remain valid until the negation of ACK at the end of the last handshake.

11.1.5.1 Asynchronous Information Transfer

The target shall control the direction of information transfer by means of the I/O signal. When I/O is true, information shall be transferred from the target to the initiator. When I/O is false, information shall be transferred from the initiator to the target.

If I/O is true (transfer to the initiator), the target shall first drive DB(7-0,P) to their desired values, delay at least one deskew delay plus a cable skew delay, then assert REQ. DB(7-0,P) shall remain valid until ACK is true at the target. The initiator shall read DB(7-0,P) after REQ is true, then signal its acceptance of the data by asserting ACK. When ACK becomes true at the target, the target may change or release DB(7-0,P) and shall negate REQ. After REQ is false the initiator shall then negate ACK. After ACK is false the target may continue the transfer by driving DB(7-0,P) and asserting REQ, as described above.

If I/O is false (transfer to the target) the target shall request information by asserting REQ. The initiator shall drive DB(7-0,P) to their desired values, delay at least one deskew delay plus a cable skew delay and assert ACK. The initiator shall continue to drive DB(7-0,P) until REQ is false. When ACK becomes true at the target, the target shall read DB(7-0,P), then negate REQ. When REQ becomes false at the initiator the initiator may change or release DB(7-0,P) and shall negate ACK. The target may continue the transfer by asserting REQ, as described above.

11.1.6 COMMAND Phase

The COMMAND phase allows the target to request command information from the initiator.

The target shall assert the C/D signal and negate the I/O and MSG signals during the REQ/ACK handshake(s) of this phase.

11.1.7 Data Phase

The data phase is a term that encompasses both the DATA IN phase and the DATA OUT phase.

11.1.7.1 DATA IN Phase

The DATA IN phase allows the target to request that data be sent to the initiator from the target.

11.1.7.2 DATA OUT Phase

The DATA OUT phase allows the target to request that data be sent from the initiator to the target.

11.1.8 STATUS Phase

The STATUS phase allows the target to request that status information be sent from the target to the initiator.

The target shall assert C/D and I/O and negate the MSG signal during the REQ/ACK handshake of this phase.

11.1.9 Message Phase

The message phase is a term that references either a MESSAGE IN, or a MESSAGE OUT phase. Multiple messages may be sent during either phase. The first byte transferred in either of these phases shall be either a single-byte message or the first byte of a multiple-byte message. Multiple-byte messages shall be wholly contained within a single message phase.

11.1.9.1 MESSAGE IN Phase

The MESSAGE IN phase allows the target to request that message(s) be sent to the initiator from the target.

The target shall assert C/D, I/O, and MSG during the REQ/ACK handshake(s) of this phase.

11.1.9.2 MESSAGE OUT Phase

The MESSAGE OUT phase allows the target to request that message(s) be sent from the initiator to the target. The target may invoke this phase at its convenience in response to the ATTENTION condition created by the initiator.

The target shall assert C/D and MSG and negate I/O during the REQ/ACK handshake(s) of this phase.

The target shall handshake byte(s) in this phase until ATN goes false.

11.1.10 Signal Restrictions Between Phases

When the SCSI bus is between two information transfer phases, the following restrictions shall apply to the SCSI bus signals:

- (1) The BSY, SEL, REQ, and ACK signals shall not change.
- (2) The C/D, I/O, MSG, and DATA BUS signals may change. When switching the DATA BUS direction from out (initiator driving) to in (target driving), the target shall delay driving the DATA BUS by at least a data release delay plus a bus settle delay after asserting the I/O signal and the initiator shall release the DATA BUS no later than a data release delay after the transition of the I/O signal to true. When switching the DATA BUS direction from in (target driving) to out (initiator driving), the target shall release the DATA BUS no later than a deskew delay after negating the I/O signal.
- (3) The ATN and RST signals may change as defined under the descriptions for the ATTENTION condition and RESET condition.

11.2 SCSI Bus Conditions

The SCSI bus has two asynchronous conditions; the ATTENTION condition and the RESET condition. These conditions cause the SCSI device to perform certain actions and can alter the phase sequence.

11.2.1 ATTENTION Condition

The ATTENTION condition allows an initiator to inform a target that the initiator has a message ready. The target may get this message during the ARBITRATION or BUS FREE phases.

The initiator creates the ATTENTION condition by asserting ATN at any time except during the ARBITRATION or BUS FREE phases.

The target may respond with the MESSAGE OUT phase.

The initiator shall keep ATN asserted if more than one byte is to be transferred. The initiator may negate the ATN signal at any time except it shall not negate the ATN signal while the ACK signal is asserted during a MESSAGE OUT phase. Normally, the initiator negates ATN while REQ is true and ACK is false during the last REQ/ACK handshake of the MESSAGE OUT phase.

11.2.2 RESET Condition

The RESET condition is used to immediately clear all SCSI devices from the bus. This condition shall take precedence over all other phases and conditions. Any SCSI device may create the RESET condition by asserting RST for a minimum of a reset hold time. During the RESET condition, the state of all SCSI bus signals other than RST is not defined.

All SCSI devices shall release all SCSI bus signals (except RST) within a bus clear delay of the transition of RST to true. The BUS FREE phase always follows the RESET condition.

11.2.2.1 "Hard" RESET Option

The RO 650 implements the "hard" RESET option. Upon detection of the RESET condition, the drive shall:

- (1) Clear all uncompleted commands.
- (2) Release all SCSI device reservations.
- (3) Return any SCSI device operating modes to their default conditions.

11.3 SCSI Bus Phase Sequences

The order in which phases are used on the SCSI bus follows a prescribed sequence.

In all systems, the RESET condition can abort any phase and is always followed by the BUS FREE phase. Also, any other phase can be followed by the BUS FREE phase.

11.3.1 Nonarbitrating Systems

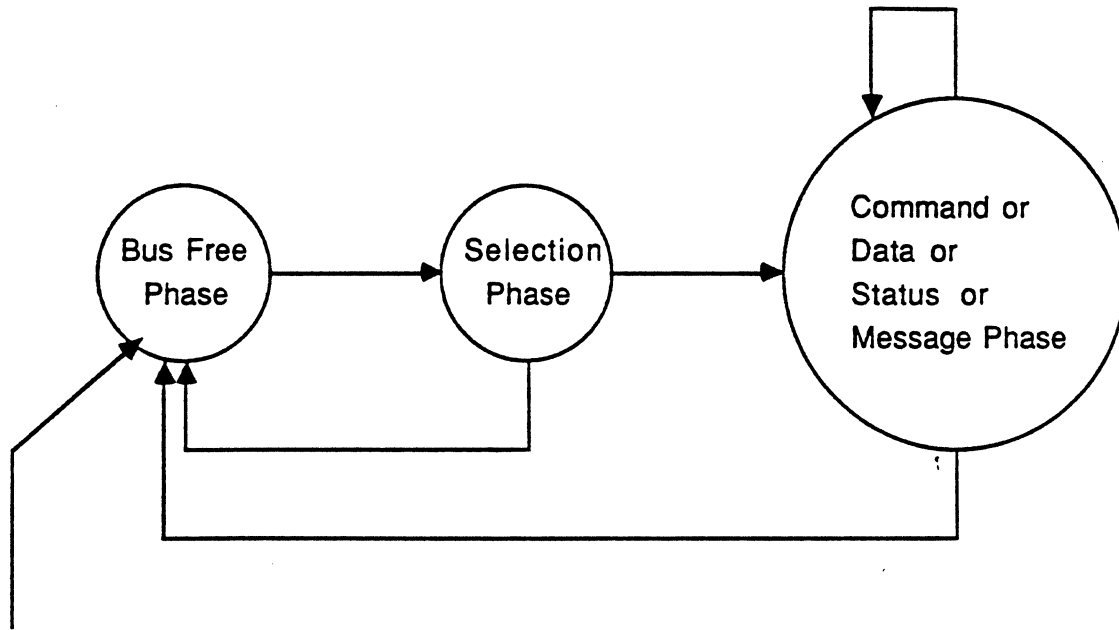
In systems where the ARBITRATION phase is not implemented, the allowable sequences shall be as shown in Figure 11.3.1. The normal progression is from the BUS FREE phase to SELECTION, and from SELECTION to one or more of the information transfer phases (COMMAND, DATA, STATUS, or MESSAGE).

11.3.2 Arbitrating Systems

In systems where the ARBITRATION phase is implemented, the allowable sequences shall be as shown in Figure 11.3.2. The normal progression is from the BUS FREE phase to ARBITRATION, from ARBITRATION to SELECTION or RESELECTION, and from SELECTION or RESELECTION to one or more of the information transfer phases (COMMAND, DATA, STATUS, or MESSAGE).

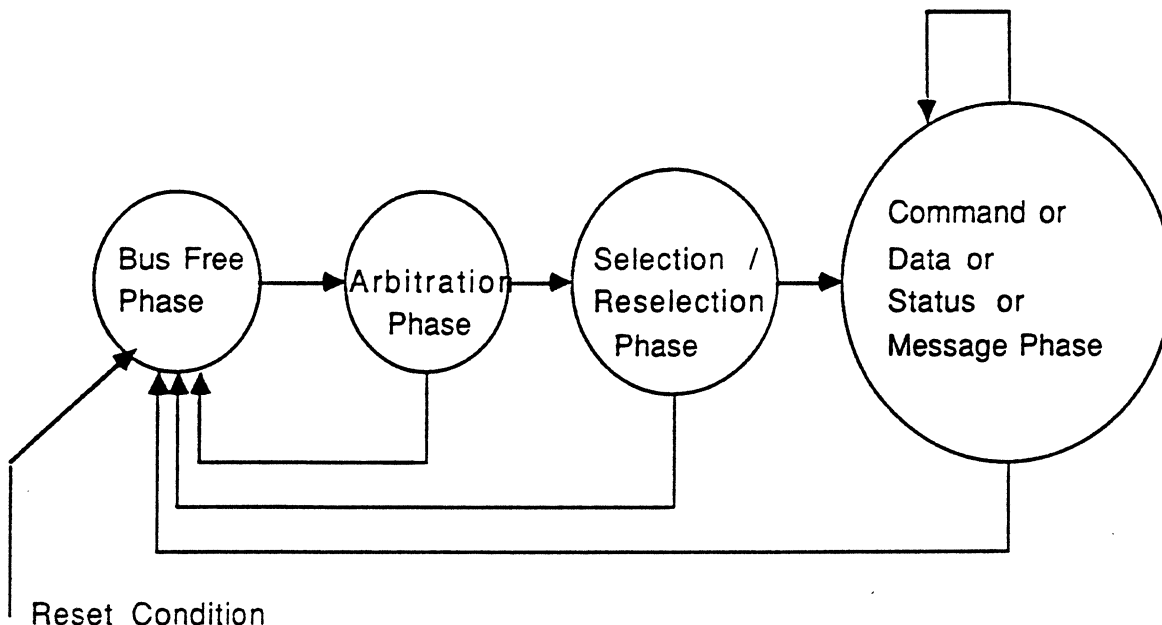
11.3.3 All Systems

There are no restrictions on the sequences between information transfer phases. A phase type may even be followed by the same phase type (eg a data phase may be followed by another data phase).



Reset Condition

FIGURE 11.3.1 : PHASE SEQUENCES WITHOUT ARBITRATION



Reset Condition

FIGURE 11.3.2 : PHASE SEQUENCES WITH ARBITRATION

11.4 SCSI Pointers

The SCSI architecture provides for two sets of three pointers within each initiator. The pointers reside in the initiator path control. The first set of pointers are known as the current (or active) pointers. These pointers are used to represent the state of the interface and point to the next command, data, or status byte to be transferred between the initiator's memory and the target. There is only one set of current pointers in each initiator. The current pointers are used by the target currently connected to the initiator.

The second set of pointers are known as the saved pointers. There is one set of saved pointers for each command that is currently active (whether or not it is currently connected). The saved command pointer always points to the start of the command descriptor block for the current command. The saved status pointer always points to the start of the status area for the current command. At the beginning of each command, the saved data pointer points to the start of the data area. It remains at this value until the target sends a SAVE DATA POINTER message to the initiator. In response to this message, the initiator stores the value of the current data pointer into the saved data pointer. The target may restore the current pointers to their saved values by sending a RESTORE POINTERS message to the initiator. The initiator moves the saved value of each pointer into the corresponding current pointer. Whenever an SCSI device disconnects from the bus, only the saved pointer values are retained. The current pointer values are restored from the saved values upon the next reconnection.

11.5 Message System Specification

The message system allows communication between an initiator and target for the purpose of physical path management.

11.5.1 Message Protocol

All SCSI devices implement the COMMAND COMPLETE message.

SCSI devices indicate their ability to accommodate more than the COMMAND COMPLETE message by asserting or responding to the ATN signal. The initiator indicates this in the SELECTION phase by asserting ATN prior to the SCSI bus condition of SEL true, and BSY false. The target indicates its ability to accommodate more messages by responding to the ATTENTION condition with the MESSAGE OUT phase after going through the SELECTION phase.

For SCSI devices that support messages other than COMMAND COMPLETE, the first message sent by the initiator after the SELECTION phase shall be the IDENTIFY message. This allows the establishment of the physical path for a particular logical unit specified by the initiator. After the RESELECTION phase, the target's first message shall be IDENTIFY. This allows the physical path to be re-established for the target's specified logical unit number. Under some exceptional conditions, an initiator may send the ABORT message or the BUS DEVICE RESET message instead of the IDENTIFY message, as the first message. Only one logical unit number shall be identified for any one selection sequence; a second IDENTIFY message with a new logical unit number shall not be issued before the SCSI bus has been released (BUS FREE phase).

Whenever a physical path is established in an initiator that can accommodate disconnection and reconnection, the initiator shall ensure that the active pointers of the physical path are equal to the saved pointers for that particular logical unit number. (An implied restore pointers operation occurs as a result of connect or reconnect.)

TABLE 11.5.2: MESSAGE CODES

Code	Type	Description	Direction	
00 _H	M	COMMAND COMPLETE	In	
02 _H	O	SAVE DATA POINTER	In	
03 _H	O	RESTORE POINTERS	In	
04 _H	O	DISCONNECT	In	
05 _H	O	INITIATOR DETECTED ERROR		Out
06 _H	O	ABORT		Out
07 _H	O	MESSAGE REJECT	In	Out
08 _H	O	NO OPERATION		Out
09 _H	O	MESSAGE PARITY ERROR		Out
0A _H	O	LINKED COMMAND COMPLETE	In	
0B _H	O	LINKED COMMAND COMPLETE (WITH FLAG)	In	
0C _H	O	BUS DEVICE RESET		Out
80 _H - FF _H	O	IDENTIFY	In	Out

KEY: In = Target to initiator
 Out = Initiator to target

11.5.2 Messages

The single byte messages supported by the RO 650 are listed along with their code values and their definitions in Table 11.5.2.

COMMAND COMPLETE 00_H

This message is sent from a target to an initiator to indicate that the execution of a command (or series of linked commands) has terminated and that valid status has been sent to the initiator.

After successfully sending this message, the target shall go to the BUS FREE phase by releasing BSY.

NOTE: The command may have been executed successfully or unsuccessfully as indicated in the status.

SAVE DATA POINTER 02_H

This message is sent from a target to direct the initiator to save a copy of the present active data pointer for the currently attached logical unit.

RESTORE POINTERS 03_H

This message is sent from a target to direct the initiator to restore the most recently saved pointers (for the currently attached logical unit) to the active state. Pointers to the command, data, and status locations for the logical unit shall be restored to the active pointers. Command and status pointers shall be restored to the beginning of the present command and status areas. The data pointer shall be restored to the value at the beginning of the data area in the absence of a SAVE DATA POINTER message or to the value at the point at which the last SAVE DATA POINTER message occurred for that logical unit.

DISCONNECT 04_H

This message is sent from a target to inform an initiator that the present physical path is going to be broken (the target plans to disconnect by releasing BSY), but that a later reconnect will be required in order to complete the current operation. If the initiator detects the BUS FREE phase (other than as a result of a RESET condition) without first receiving a DISCONNECT or COMMAND COMPLETE message, the initiator shall consider this as a catastrophic error condition. If the target intentionally creates this condition, the target shall clear the current command. This message shall not cause the initiator to save the data pointer.

Note: If DISCONNECT messages are used to break a long data transfer into two or more shorter transfers, then a SAVE DATA POINTER should be issued before each DISCONNECT message.

INITIATOR DETECTED ERROR 05_H

This message is sent from an initiator to inform a target that an error (eg parity error) has occurred that does not preclude the target from retrying the operation. Although present pointer integrity is not assured, a RESTORE POINTER message or a disconnect followed by a reconnect, shall cause the pointers to be restored to their defined prior state.

ABORT 06_H

This message is sent from the initiator to the target to clear the present operation. If a logical unit has been identified, all pending data and status for the issuing initiator from the effected logical unit shall be cleared, and the target shall go to the BUS FREE phase. Pending data and status for other initiators shall not be cleared. If a logical unit has not been identified, the target shall go to the BUS FREE phase. No status or ending message shall be sent for the operation. It is not an error to issue this message to a logical unit that is not currently performing an operation for the initiator.

MESSAGE REJECT 07_H

This message is sent from either the initiator or target to indicate that the last message it received was inappropriate or has not been implemented.

In order to indicate its intentions of sending this message, the initiator shall assert the ATN signal prior to its release of ACK for the REQ/ACK handshake of the message that is to be rejected. When a target sends this message, it shall change to MESSAGE IN phase and send this message prior to requesting additional message bytes from the initiator. This provides an interlock so that the initiator can determine which message is rejected.

NO OPERATION 08_H

This message is sent from an initiator in response to a target's request for a message when the initiator does not currently have any other valid message to send.

MESSAGE PARITY ERROR 09_H

This message is sent from the initiator to the target to indicate that one or more bytes in the last message it received had a parity error.

In order to indicate its intentions of sending this message, the initiator shall assert the ATN signal prior to its release of ACK for the REQ/ACK handshake of the message that has the parity error. This provides an interlock so that the target can determine which message has the parity error.

LINKED COMMAND COMPLETE 0A_H

This message is sent from a target to an initiator to indicate that the execution of a linked command has completed and that status has been sent. The initiator shall then set the pointers to the initial state for the next linked command.

LINKED COMMAND COMPLETE (WITH FLAG) 0B_H

This message is sent from a target to an initiator to indicate that the execution of a linked command (with the flag bit set to one) has completed and that status has been sent. The initiator shall then set the pointer to the initial state of the next linked command. Typically this message would be used to cause an interrupt in the initiator between two linked commands.

BUS DEVICE RESET 0C_H

This message is sent from an initiator to direct a target to clear all current commands on that SCSI device. This message forces the SCSI device to an initial state with no operations pending for any initiator. Upon recognizing this message, the target shall go to the BUS FREE phase.

IDENTIFY 80_H to FF_H

These messages are sent by either the initiator or the target to establish the physical path connection between an initiator and target for a particular logical unit.

Bit 7

This bit is always set to one to distinguish these messages from the other messages.

Bit 6

This bit is only set to one by the initiator. When set to one, it indicates that the initiator has the ability to accommodate disconnection and reconnection.

Bits 5-3

Reserved.

Bits 2-0

These bits specify a logical unit number in a target.

Only one logical unit number shall be identified for any one selection sequence; a second IDENTIFY message with a new logical unit number shall not be issued before the bus has been released (BUS FREE phase).

When sent from a target to an initiator during reconnection, an implied RESTORE POINTERS message shall be performed by the initiator prior to completion of this message.

11.6 Status

A status byte shall be sent from the target to the initiator during the STATUS phase at the termination of each command as specified in Tables 11.6.1 and 11.6.2 unless the command is cleared by an ABORT message, by a BUS DEVICE RESET message, or by a "hard" RESET condition.

TABLE 11.6.1 : STATUS BYTE

Bit	7	6	5	4	3	2	1	0
Byte								
0	Reserved			Status Byte Code				0

TABLE 11.6.2 : STATUS BYTE CODE BIT VALUES

Bits of Status Byte					Status Represented
4	3	2	1	0	
0	0	0	0	0	GOOD
0	0	0	1	0	CHECK CONDITION
0	1	0	0	0	BUSY
1	0	0	0	0	INTERMEDIATE/GOOD
1	1	0	0	0	RESERVATION CONFLICT

A description of the status byte codes is given below:

GOOD

This status indicates that the target has successfully completed the command.

CHECK CONDITION

Any error, exception, or abnormal condition that causes sense data to be set, shall cause a CHECK CONDITION status. The REQUEST SENSE command should be issued following a CHECK CONDITION status, to determine the nature of the condition.

BUSY

The target is busy. This status shall be returned whenever a target is unable to accept a command from an initiator. The normal initiator recovery action is to issue the command again at a later time.

INTERMEDIATE

This status shall be returned for every command in a series of linked commands (except the last command), unless an error, exception, or abnormal condition causes a CHECK CONDITION status or a RESERVATION CONFLICT status to be set. If this status is not returned, the chain of linked commands is broken, no further commands in the series are executed.

RESERVATION CONFLICT

This status shall be returned whenever an SCSI device attempts to access a logical unit or an extent within a logical unit that is reserved for that type of access to another SCSI device.

12.0 SCSI Commands

This section defines the SCSI command structure and gives several examples.

The command definitions assume a data structure providing the appearance at the interface of a contiguous set of logical blocks of a fixed or explicitly defined data length. The SCSI device maps the physical characteristics of the attached peripheral devices to one of several logical structures defined by the device type code.

A single command may transfer one or more logical blocks of data. Multiple commands may be linked if they are sent to the same logical unit. A target may disconnect from the SCSI bus to allow activity by other SCSI devices while a logical unit is being prepared to transfer data.

Upon command completion (successful or unsuccessful), the target returns a status byte to the initiator. Since most error and exception conditions cannot be adequately described with a single status byte, one status code, CHECK CONDITION, indicates that additional information is available. The initiator may issue a REQUEST SENSE command to retrieve this additional information.

12.1 Command Implementation Requirements

The first byte of any SCSI command shall contain an operation code as defined in this document. Three bits (bits 7 - 5) of the second byte of each SCSI command specify the logical unit if it is not specified using the IDENTIFY message. The last byte of all SCSI commands shall contain a control byte as defined in 12.2.6.

12.1.1 Reserved

Reserved bits, fields, bytes, and code values are set aside for future standardization. A reserved bit, field, or byte shall be set to zero. A target that receives a reserved bit, field, or byte that is not zero or receives a reserved code value shall terminate the command with a CHECK CONDITION status and, if extended sense is implemented, the sense key shall be set to ILLEGAL REQUEST.

12.1.2 Unit Attention Condition

A unit attention condition for a logical unit shall begin for each initiator whenever the target has been reset (by a BUS DEVICE RESET message or a "hard" RESET condition). The unit attention condition shall persist for each initiator until that initiator issues a command to the logical unit other than REQUEST SENSE or INQUIRY for which the target shall return CHECK CONDITION status. If the next command from that initiator to the logical unit (following the CHECK CONDITION status) is REQUEST SENSE, then the UNIT ATTENTION sense key shall be returned. (If any command other than REQUEST SENSE is received, the unit attention condition is lost.)

If an INQUIRY command is received from an initiator with a pending unit attention condition (before the target reports CHECK CONDITION status), the target shall perform the INQUIRY command and shall not clear the unit attention condition.

If a REQUEST SENSE command is received from an initiator with a pending unit attention condition (before the target reports CHECK CONDITION status), then the target shall clear the unit attention condition for that initiator.

If an initiator issues a command other than INQUIRY or REQUEST SENSE while a unit attention condition exists for that initiator, the target shall not perform the command and shall report CHECK CONDITION status.

12.2 Command Descriptor Block

A request to a peripheral device is performed by sending a command descriptor block to the target. For several commands, the request is accompanied by a list or parameters sent during the DATA OUT phase. See the specific commands for detailed information.

The command descriptor block always has an operation code as the first byte of the command. This is followed by a logical unit number, command parameters (if any), and a control byte.

For all commands, if there is an invalid parameter in the command descriptor block, then the target shall terminate the command without altering the medium.

12.2.1 Operation Code

The operation code (Table 12.2.1) of the command descriptor block has a group code field and a command code field. The three-bit group code field provides for eight groups of command codes in each group. Thus, a total of 256 possible operation codes exist.

The group code specifies one of the following groups:

- Group 0 - six-byte commands
- Group 1 - ten-byte commands
- Group 2 - reserved
- Group 3 - reserved
- Group 4 - reserved
- Group 5 - twelve-byte commands
- Group 6 - vendor unique
- Group 7 - vendor unique

TABLE 12.2.1 : OPERATION CODE

Bit	7	6	5	4	3	2	1	0
Byte								
0	Group Code			Command Code				

TABLE 12.2.2 : TYPICAL COMMAND DESCRIPTOR BLOCK FOR SIX-BYTE COMMANDS

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Logical Block Address (if required) (MSB)				
2	Logical Block Address (if required)							
3	Logical Block Address (if required) (LSB)							
4	Transfer Length (if required)							
5	Control Byte							

TABLE 12.2.3 : TYPICAL COMMAND DESCRIPTOR BLOCK FOR TEN-BYTE COMMANDS

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved				RelAdr
2	Logical Block Address (if required) (MSB)							
3	Logical Block Address (if required)							
4	Logical Block Address (if required)							
5	Logical Block Address (if required) (LSB)							
6	Reserved							
7	Transfer Length (if required) (MSB)							
8	Transfer Length (if required) (LSB)							
9	Control Byte							

12.2.2 Logical Unit Number

The logical unit number addresses one of up to eight physical or virtual devices attached to a target. This method of addressing is provided for systems that do not implement the IDENTIFY message. A target that accepts an IDENTIFY message shall use the logical unit number specified within the message. In this case, the target shall ignore the logical unit number specified within the command descriptor block. The LUN must be zero for the RO 650.

12.2.3 Logical Block Address

The logical block address on logical units shall begin with block zero and be contiguous up to the last logical block on that logical unit.

Group 0 command descriptor blocks contain 21-bit logical block addresses. Groups 1 and 5 command descriptor blocks contain 32-bit logical block addresses.

The logical block concept implies that the initiator and target shall have previously established the number of data bytes per logical block. This may be established through the use of the READ CAPACITY command or the MODE SENSE command.

12.2.4 Relative Address Bit

The relative address (RelAdr) bit of the group 1 and group 5 commands is set to one to indicate that the logical block address portion of the command descriptor block is a two's complement displacement. This negative or positive displacement is to be added to the logical block address last accessed on the logical unit to form the logical block address for this command. This feature is only available when linking commands. The feature requires that a previous command in the linked group have accessed a block of data on the logical unit. The relative address bit is not supported by the RO 650.

12.2.5 Transfer Length

The transfer length specifies the amount of data to be transferred, usually the number of blocks. For several commands the transfer length indicates the requested number of bytes to be sent as defined in the command description. For these commands the transfer length field may be identified by a different name. See the following descriptions and the individual command descriptions for further information.

Commands that use one byte for transfer length allow up to 65,535 blocks of data to be transferred by one command. A transfer length value of 1 to 255 indicates the number of blocks that shall be transferred. A value of zero indicates 256 blocks.

Commands that use two bytes for transfer length allow up to 65,535 blocks of data to be transferred by one command. In this case, a transfer length of zero indicates that no data transfer shall take place. A value of 1 to 65,535 indicates the number of blocks that shall be transferred.

For several commands more than two bytes are allocated for transfer length. Refer to the specific command description for further information.

The transfer length of the commands that are used to send a list of parameters to a target is called the parameter list length. The parameter list length specifies the number of bytes sent during the DATA OUT phase.

The transfer length of the commands that are used to return sense data (eg REQUEST SENSE, INQUIRY, MODE SENSE, etc) to an initiator is called the allocation length. The allocation length specifies the number of bytes that the initiator has allocated for returned data. The target shall terminate the DATA IN phase when allocation length bytes have been transferred or when all available sense data have been transferred to the initiator, whichever is less.

12.2.6 Control Byte

The control byte is the last byte of every command descriptor block. A typical control byte is described in Table 12.2.6.

TABLE 12.2.6: CONTROL BYTE

Bit	7	6	5	4	3	2	1	0
Byte								
Last	Vendor unique			Reserved			Flag	Link

BIT DESCRIPTION

7 - 6 Vendor unique

5 - 2 Reserved

1 Flag bit - If the link bit is zero, then the flag bit shall be set to zero. If the link bit is one, and if the command terminates successfully, the target shall send LINKED COMMAND COMPLETE message if the flag bit is zero and shall send LINKED COMMAND COMPLETE (WITH FLAG) message if the flag bit is one. Typically, this bit is used to cause an interrupt in the initiator between linked commands.

0 Link bit - This bit is set to one to indicate that the initiator desires an automatic link to the next command upon successful completion of the current command. If the link bit is one, the target, upon successful termination of the command, shall return INTERMEDIATE status and shall then send one of the two messages defined by the flag bit (above).

13.0 RO 650 SCSI COMMAND DESCRIPTIONSTABLE 13.0 : COMMAND SUMMARY

<u>OPERATION CODE (HEX)</u>	<u>COMMAND NAME</u>
00	TEST UNIT READY
01	REZERO UNIT
03	REQUEST SENSE
04	FORMAT UNIT
07	REASSIGN BLOCKS
08	READ
0A	WRITE
0B	SEEK
12	INQUIRY
15	MODE SELECT
16	RESERVE UNIT
17	RELEASE UNIT
1A	MODE SENSE
1B	START/STOP UNIT
1D	SEND DIAGNOSTIC
25	READ CAPACITY
28	READ EXTENDED
2A	WRITE EXTENDED
2F	VERIFY
37	READ DEFECT DATA
3B	WRITE BUFFER
3C	READ BUFFER
	E0 MAINTENANCE SEEK
(These commands	E1 FORMAT MAINTENANCE TRACKS
are Group 7	E2 CERTIFY
VENDOR UNIQUE	E8 FAST READ
and intended for	EA FAST WRITE
factory use only)	EB READ RESERVATIONS
	EF REGISTER TEST

13.1 TEST UNIT READY Command

Operation Code: 00H

TABLE 13.1 : TEST UNIT READY COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved				
2	Reserved							
3	Reserved							
4	Reserved							
5	Reserved					Flag	Link	

The TEST UNIT READY command checks that the drive is ready.

If the drive is ready, the command will return GOOD status.

If the drive is not ready, the command will return CHECK CONDITION status. A REQUEST SENSE command will return a sense key of 02H with an error code of 00H.

13.2 REZERO UNIT CommandOperation Code: 01_HTABLE 13.2 : REZERO UNIT COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved				
2	Reserved							
3	Reserved							
4	Reserved							
5	Reserved					Flag	Link	

The REZERO UNIT command positions the read/write heads over track zero.

If this operation is successful, the command will return GOOD status.

If this operation is unsuccessful, the command will return CHECK CONDITION status. A REQUEST SENSE command will return a sense key of 04H with an error code of 06H. The drive will shut down the spindle and stepper motors. This is a fatal error; no further commands will be executed and the drive will return CHECK CONDITION status to all commands.

13.3 REQUEST SENSE CommandOperation Code: 03_HTABLE 13.3 : REQUEST SENSE COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved				
2	Reserved							
3	Reserved							
4	Allocation Length							
5	Reserved					Flag		Link

The REQUEST SENSE command requests that the target transfer sense data to the initiator.

The sense data shall be valid for a CHECK CONDITION status returned on the prior command. This sense data shall be preserved by the target for the initiator until retrieved by the REQUEST SENSE command or until the receipt of any other command from the initiator that issued the command resulting in the CHECK CONDITION status. Sense data shall be cleared upon receipt of any subsequent command to the target from the initiator option, the target shall assume that the REQUEST SENSE command is from the same initiator.

The allocation length specifies the number of bytes that the initiator has allocated for returned sense data. An allocation length of zero indicates that four bytes of sense data shall be transferred. Any other value indicates the maximum number of bytes that shall be transferred. The target shall return the number of sense bytes allocated up to a maximum of 18 bytes.

NOTE: No error condition will be created by asking for too few or too many sense bytes.

The REQUEST SENSE command shall return the CHECK CONDITION status only to report fatal errors for the REQUEST SENSE command. For example:

- (1) The target receives a nonzero reserved bit in the command descriptor.
- (2) An unrecovered parity error occurs on the DATA BUS.
- (3) A target malfunction prevents return of the sense data.

If any nonfatal error occurs on a REQUEST SENSE command, the target shall return the sense data with GOOD status.

Following a fatal error on a REQUEST SENSE command, sense data may be invalid.

13.3.1 Nonextended Sense

The format of the sense data is determined by the error class. Error classes 0 through 6 use the nonextended sense data format.

The RO 650 does not implement nonextended sense.

13.3.2 Extended Sense

Error class 7 specifies extended sense. Error code zero specifies the extended sense data format.

The extended sense data format is shown in Table 13.3.2.

TABLE 13.3.2 : EXTENDED SENSE DATA FORMAT

Bit	7	6	5	4	3	2	1	0
Byte								
0	Valid	Error Class (7)			Error Code (0)			
1	Reserved							
2	Reserved				Sense Key			
3	Information Byte (MSB)							
4	Information Byte							
5	Information Byte							
6	Information Byte (LSB)							
7	Additional Sense Length (n)							
8 - 17	Additional Sense Bytes							

The information bytes are not defined if the valid bit is zero. If the valid bit is one, the information bytes contain the unsigned logical block address associated with the sense key.

The sense keys are described in Table 13.3.3.

The additional sense length specifies the number of additional sense bytes to follow. If the allocation length of the command descriptor block is too small to transfer all of the additional sense bytes, the additional sense length is not adjusted to reflect the truncation. The additional sense length is set to OAH.

The additional sense bytes contain an additional sense code in byte 12 and zeros in the remaining bytes. The additional sense codes are described in Table 13.3.4.

TABLE 13.3.3 : SENSE KEY DESCRIPTIONS

<u>Sense Key</u>	<u>Description</u>
0 _H	NO SENSE. Indicates that there is no specific sense key information to be reported for the designated logical unit.
1 _H	RECOVERED ERROR. Indicates that the last command completed successfully with some recovery action performed by the target. Details may be determinable by examining the additional sense bytes and the information bytes.
2 _H	NOT READY. Indicates that the target cannot be accessed. Operator intervention may be required to correct this condition. :
3 _H	MEDIUM ERROR. Indicates that the command terminated with a nonrecovered error condition that was probably caused by a flaw in the medium or an error in the recorded data.
4 _H	HARDWARE ERROR. Indicates that the target detected a nonrecoverable hardware failure while performing the command or during a self test.
5 _H	ILLEGAL REQUEST. Indicates that there was an illegal parameter in the command descriptor block or in the additional parameters supplied as data for some commands. If the target detects an invalid parameter in the command descriptor block, then it shall terminate the command without altering the medium. If the target detects an invalid parameter in the additional parameters supplied as data, then the target may have already altered the medium.
6 _H	UNIT ATTENTION. Indicates that the target has been reset.
B _H	ABORTED COMMAND. Indicates that the target aborted the command.

TABLE 13.3.4 : ADDITIONAL SENSE CODE DESCRIPTIONS

<u>SENSE</u> <u>CODE (HEX)</u>	<u>DESCRIPTION</u>	<u>RELATED</u> <u>SENSE KEY</u>
00	NO ADDITIONAL SENSE INFORMATION	NO SENSE
03	WRITE FAULT	HARDWARE ERROR
04	DRIVE NOT READY	NOT READY
06	NO TRACK ZERO FOUND	HARDWARE ERROR
10	ID ECC ERROR	MEDIUM ERROR
11	UNRECOVERED DATA ERROR	MEDIUM ERROR
12	NO ID ADDRESS MARK	MEDIUM ERROR
13	NO DATA ADDRESS MARK	MEDIUM ERROR
14	RECORD NOT FOUND	MEDIUM ERROR
15	SEEK ERROR	MEDIUM ERROR
17	RECOVERED READ ERROR BY RETRIES	RECOVERED ERROR
18	RECOVERED READ ERROR BY ECC	RECOVERED ERROR
19	DEFECT LIST ERROR	MEDIUM ERROR
1A	PARAMETER OVERRUN	ILLEGAL REQUEST
1C	DEFECT LIST NOT FOUND	MEDIUM ERROR
20	INVALID COMMAND	ILLEGAL REQUEST
21	ILLEGAL BLOCK ADDRESS	ILLEGAL REQUEST
22	ILLEGAL FUNCTION	ILLEGAL REQUEST
24	ILLEGAL FIELD IN CDB	ILLEGAL REQUEST
25	INVALID LUN	ILLEGAL REQUEST
26	INVALID FIELD IN PARAMETER LIST	ILLEGAL REQUEST
29	POWER ON OR RESET OR BUS DEVICE RESET OCCURRED	UNIT ATTENTION
2A	MODE SELECT PARAMETERS CHANGED	UNIT ATTENTION
31	FORMAT CORRUPTED	MEDIUM ERROR
32	NO DEFECT SPARE LOCATION AVAILABLE	MEDIUM ERROR
40	RAM DIAGNOSTIC FAILURE	HARDWARE ERROR
43	MESSAGE REJECT ERROR	ABORTED COMMAND
47	PARITY ERROR	ABORTED COMMAND
48	INITIATOR DETECTED ERROR	ABORTED COMMAND
80	SPINDLE MOTOR FAILED TO START	HARDWARE ERROR
81	SPINDLE MOTOR SPEED ERROR $\pm 1\%$	HARDWARE ERROR
82	SPINDLE MOTOR SPEED ERROR $\pm 5\%$	HARDWARE ERROR
83	INDEX CALIBRATION FAILED	HARDWARE ERROR
84	ECC DIAGNOSTICS FAILED	HARDWARE ERROR
85	R/W DIAGNOSTICS FAILED	HARDWARE ERROR
86	ROM DIAGNOSTICS FAILED	HARDWARE ERROR
87	SEEK DIAGNOSTICS FAILED	HARDWARE ERROR
88	RECAL DIAGNOSTICS FAILED	HARDWARE ERROR
89	INTERFACE DIAGNOSTICS FAILED	HARDWARE ERROR

13.4 FORMAT UNIT CommandOperation Code: 04_HTABLE 13.4.1 : FORMAT UNIT COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			FmtData	CmpLst	Defect List Format		
2	Reserved							
3	Interleave (MSB)							
4	Interleave (LSB)							
5	Reserved						Flag	Link

The FORMAT UNIT command writes all ID and data fields with the format specified by a previous MODE SELECT command. The drive is shipped with a format of 532 byte sectors and a 1 : 1 interleave.

The RO 650A combines the Format Data (FMTDATA), Complete List (CMPLST) and Defect List Format bits into a five bit Format Control Code. This code defines how the FORMAT UNIT command deals with defect lists as defined in section 14.0 DEFECT HANDLING. See Table 13.4.2.

The Interleave Field requests that the logical blocks be related in a specific fashion to physical blocks. An interleave value of zero requests that the target use its default interleave. An interleave value of one requests that consecutive logical blocks be placed in consecutive physical order. Values of two and one less than the total number of sectors in a track results in interleaved formatting. If the interleave value does not fall within the above range a CHECK CONDITION status will be returned.

The FORMAT UNIT command shall be rejected with RESERVATION CONFLICT status if any extent in the unit is reserved.

TABLE 13.4.2 : FORMAT CONTROL CODE DESCRIPTION

<u>FORMAT CONTROL CODE (HEX)</u>	<u>DESCRIPTION</u>
00 or 10	Format the drive using the Primary Defect List (PLIST) which was written on the drive during manufacture and include the Growing Defect List (GLIST).
18	Format the drive using the Primary Defect List (PLIST) only. Any GLIST will be deleted and not used.
1E	Format the drive and input the PLIST during the DATA OUT phase. This command should only be issued during drive manufacture.
16	Used to input the PLIST but no format operation takes place.

A defect list shall be supplied to the target during the DATA OUT phase. Format Control Code 00H has no DATA OUT phase, while Format Control Codes 10H and 18H require a Defect List Header with the Defect List Length set to 0000H. See Table 13.4.3.

TABLE 13.4.3 : DEFECT LIST

Byte		Defect List Header	
0		Reserved	
1		Reserved	
2		Defect List Length (MSB)	
3		Defect List Length (LSB)	
		Defect Descriptor(s)	
0		Cylinder Number of Defect (MSB)	
1		Cylinder Number of Defect	
2		Cylinder Number of Defect (LSB)	
3		Head Number of Defect	
4		Defect Bytes from Index (MSB)	
5		Defect Bytes from Index	
6		Defect Bytes from Index	
7		Defect Bytes from Index (LSB)	

Each defect descriptor specifies the beginning of an eight-byte defect location on the medium. Each defect descriptor is comprised of the cylinder number of defect, the head number of defect, and the defect bytes from index. The defect descriptors shall be in ascending order. For determining ascending order, the cylinder number of defect is considered the most significant part of the address and the defect bytes from index is considered the least significant part of the address.

13.5 REASSIGN BLOCKS CommandOperation Code: 07_HTABLE 13.5.1 : REASSIGN BLOCKS COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number				Reserved			
2	Reserved							
3	Reserved							
4	Reserved							
5	Reserved						Flag	Link

The REASSIGN BLOCKS command requests the target to reassign the defective logical blocks to an area on the logical unit reserved for this purpose.

The initiator transfers a defect list that contains the logical block addresses to be reassigned. The target shall reassign the physical medium used for each logical block address in the list. The data contained in the logical blocks specified in the defect list may be altered, but the data in all other logical blocks on the medium shall be preserved.

The effect of specifying a logical block to be reassigned that previously has been reassigned is to reassign the block again. Thus, over the life of the medium, a logical block can be reassigned to multiple physical addresses (until no more spare locations remain on the medium).

The REASSIGN BLOCKS defect list contains a four-byte header followed by one or more defect descriptors. The length of each defect descriptor is four bytes.

The defect list length specifies the total length in bytes of the defect descriptors that follow. The defect list length is equal to four times the number of defect descriptors.

TABLE 13.5.2 : REASSIGN BLOCKS DEFECT LIST

Byte		Defect List Header	
0		Reserved	
1		Reserved	
2		Defect List Length (MSB)	
3		Defect List Length (LSB)	
		Defect Descriptor(s)	
0		Defect Logical Block Address (MSB)	
1		Defect Logical Block Address	
2		Defect Logical Block Address	
3		Defect Logical Block Address (LSB)	

The defect descriptor specifies a four-byte defect logical block address that contains the defect. The defect descriptors shall be in ascending order.

If the drive has insufficient capacity to reassign all of the defective logical blocks, the command shall terminate with a CHECK CONDITION status and the sense key shall be set to MEDIUM ERROR. The logical block address of the first logical block not reassigned shall be returned in the information bytes of the sense data.

13.6 READ CommandOperation Code: 08_HTABLE 13.6 : READ COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Logical Block Address (MSB)				
2	Logical Block Address							
3	Logical Block Address (LSB)							
4	Transfer Length							
5	Reserved						Flag	Link

The READ command requests that the target transfer data to the initiator.

The logical block address specifies the logical block at which the read operation shall begin.

The transfer length specifies the number of contiguous logical blocks of data to be transferred. A transfer length of zero indicates that 256 logical blocks shall be transferred. Any other value indicates the number of logical blocks that shall be transferred.

The most recent data value written in the addressed logical block shall be returned.

This command shall be terminated with a RESERVATION CONFLICT status if any reservation access conflict exists and no data shall be read.

If any of the following conditions occur, this command shall be terminated with a CHECK CONDITION status, and the sense key shall be set as indicated in the following table.

CONDITIONSENSE KEY

Invalid logical block address

ILLEGAL REQUEST (see note)

Target reset since last command from
this initiator

UNIT ATTENTION

Unrecoverable read error

MEDIUM ERROR

Overrun or other error that might be
resolved by repeating the command

ABORTED COMMAND

NOTE: The extended sense information bytes shall be set to the logical block address
of the first invalid address.

13.7 WRITE CommandOperation Code: 0A_HTABLE 13.7 : WRITE COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							:
1	Logical Unit Number			Logical Block Address (MSB)				
2	Logical Block Address							
3	Logical Block Address (LSB)							
4	Transfer Length							
5	Reserved						Flag	Link

The WRITE command requests that the target write the data transferred by the initiator to the medium.

The logical block address specifies the logical block at which the write operation shall begin.

The transfer length specifies the number of contiguous logical blocks of data to be transferred. A transfer length of zero indicates that 256 logical blocks shall be transferred. Any other value indicates the number of logical blocks that shall be transferred.

This command shall be terminated with a RESERVATION CONFLICT status if any reservation access conflict exists and no data shall be written.

If any of the following conditions occur, this command shall be terminated with a CHECK CONDITION status, and the sense key shall be set as indicated in the following table.

CONDITION

SENSE KEY

Invalid logical block address

ILLEGAL REQUEST (see note)

Target reset since last command from
this initiator

UNIT ATTENTION

Overrun or other error that might be
resolved by repeating the command

ABORTED COMMAND

NOTE: The extended sense information bytes shall be set to the logical block address of the first invalid address. In this case, no data shall be written on the logical unit.

13.8 SEEK CommandOperation Code: 0B_HTABLE 13.8 : SEEK COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Logical Block Address (MSB)				
2	Logical Block Address							
3	Logical Block Address (LSB)							
4	Reserved							
5	Reserved						Flag	Link

The SEEK command requests that the logical unit seek to the specified logical block address.

13.9 INQUIRY CommandOperation Code: 12_HTABLE 13.9.1 : INQUIRY COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved				
2	Reserved							
3	Reserved							
4	Allocation Length							
5	Reserved					Flag	Link	

The INQUIRY command requests that information regarding parameters of the target be sent to the initiator.

The allocation length specifies the number of bytes that the initiator has allocated for returned INQUIRY data. An allocation length of zero indicates that no INQUIRY data shall be transferred. This condition shall not be considered as an error. Any other value indicates the maximum number of bytes that shall be transferred. The target shall terminate the DATA IN phase when allocation length bytes have been transferred or when all available INQUIRY data have been transferred to the initiator, whichever is less.

The INQUIRY command shall return a CHECK CONDITION status only when the target cannot return the requested INQUIRY data.

If an INQUIRY command is received from an initiator with a pending unit attention condition (before the target reports CHECK CONDITION status), the target shall perform the INQUIRY command and shall not clear the unit attention condition.

The INQUIRY data (Table 13.9.2) contains a five byte header, followed by the data as shown in Table 13.9.3 additional bytes description.

TABLE 13.9.2 : INQUIRY DATA

Bit	7	6	5	4	3	2	1	0
Byte								
0	Peripheral Device Type (00)							
1	RMB (0) Device-Type Qualifier (00)							
2	ISO Version (0)		ECMA Version (0)			ANSI Version (0)		
3	Reserved				Response Data Format (1)			
4	Additional Length (31)							

TABLE 13.9.3 : ADDITIONAL BYTES DESCRIPTION

Byte 5	00		
Byte 6	00		
Byte 7	00		
Byte 8	52H	'R'	
Byte 9	4FH	'O'	
Byte 10	44H	'D'	
Byte 11	49H	'I'	VENDOR IDENTIFICATION
Byte 12	4DH	'M'	
Byte 13	45H	'E'	
Byte 14	20H	' '	
Byte 15	20H	' '	
Byte 16	52H	'R'	
Byte 17	4FH	'O'	
Byte 18	36H	'6'	
Byte 19	33H	'3'	
Byte 20	32H	'2'	
Byte 21	20H	' '	
Byte 22	20H	' '	
Byte 23	20H	' '	PRODUCT
Byte 24	20H	' '	IDENTIFICATION
Byte 25	20H	' '	
Byte 26	20H	' '	
Byte 27	20H	' '	
Byte 28	20H	' '	
Byte 29	20H	' '	
Byte 30	20H	' '	
Byte 31	20H	' '	
Byte 32	3XH		
Byte 33	2EH		FIRMWARE REVISION LEVEL
Byte 34	3XH		
Byte 35	3XH		
Byte 36	Number of extents MSB		
Byte 37	Number of extents LSB		
Byte 38	OOH Class 0 Command List		

Byte 39	Bit Map of supported commands 0H-7H
Byte 40	Bit Map of supported commands 8H-0FH
Byte 41	Bit Map of supported commands 10H-17H
Byte 42	Bit Map of supported commands 18H-1FH
Byte 43	01H Class 1 command list
Byte 44	Bit Map of supported commands 0H-7H
Byte 45	Bit Map of supported commands 8H-0FH
Byte 46	Bit Map of supported commands 10H-17H
Byte 47	Bit Map of supported commands 18H-1FH
Byte 48	07H Class 7 command list
Byte 49	Bit Map of supported commands 0H-7H
Byte 50	Bit Map of supported commands 8H-0FH
Byte 51	Bit Map of supported commands 10H-17H
Byte 52	Bit Map of supported commands 18H-1FH
Byte 53	FFH (End of List)

13.10 MODE SELECT CommandOperation Code: 15_HTABLE 13.10.1 : MODE SELECT COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved				SP
2	Reserved							
3	Reserved							
4	Parameter List Length							
5	Reserved						Flag	Link

The MODE SELECT command provides a means for the initiator to specify medium, logical unit, or peripheral device parameters to the target.

SP (Save Parameters) bit 0 byte 1 set to one indicates that the target shall:

- update the Current mode values with the values defined in the following Pages;
- save all Saveable Pages except the Pages defined by the Page Codes 3, 4 and 5 which are to be saved during the next successfully completed FORMAT UNIT command...
- then report Command Complete with no CHECK CONDITION status when successfully completing the above.

Saveable Pages are Pages for which preceding MODE SENSE commands returned the PS bit (bit 7 byte 0) of the Page Header set to one.

SP bit 0 byte 1 set to zero indicates that the target shall:

- update the Current mode values with the values defined in the following Pages;
- shall not save the Saveable Pages;
- shall not modify the saved parameters of the Pages defined by the Page Codes 3, 4 and 5.
- then shall report Command Complete with no CHECK CONDITION status when successfully completing the above.

The parameter list length specifies the length in bytes of the MODE SELECT parameter list that shall be transferred during the DATA OUT phase. A parameter list length of zero indicates that no data shall be transferred. This condition shall not be considered as an error.

The MODE SELECT parameter list (Table 13.10.2) contains a four-byte header, followed by zero or more block descriptions, followed by zero or more Pages.

TABLE 13.10.2: MODE SELECT PARAMETER LIST

<u>BYTE</u>	<u>MODE SELECT HEADER</u>
0	Reserved
1	Medium Type (00)
2	Reserved
3	Block Descriptor Length (08)
<u>BLOCK DESCRIPTOR(S)</u>	
0	Density Code (00)
1	Number of Blocks (MSB) (00)
2	Number of Blocks (00)
3	Number of Blocks (LSB) (00)
4	Reserved
5	Block Length (MSB)
6	Block Length
7	Block Length (LSB)
<u>PAGE DESCRIPTOR(S)</u>	
Bit	7 6 5 4 3 2 1 0
Byte	
0	R R Page Code
1	Page Length (in bytes)
2 to n	Refer to each Page

Optional additional blocks of parameters called "Pages" may be sent to the target in the Data Out phase of the MODE SELECT command, following either:

- the MODE SELECT Header, if the Block Descriptor length is set to zero.
- or all Block Descriptors, if the Block Descriptor length is different than zero.

The Block Descriptor Length shall not include the length of the Pages.

Each defined Page is preceded by a Header of two bytes defining the Page Code and the length of the page. Following the Header the Pages are separated into sub-blocks containing a list of related flags and/or values.

Bits 7 and 6 of byte 0 are reserved.

The Page Code identifies the meaning of the following bytes in the Page.

The Page Length indicates the number of bytes that the target supports in each Page. The Page Length value of each defined Page, shall not include the Page Length byte. The target will return in the Pages of the MODE SENSE commands as many consecutive bytes as it supports, for each Page that it supports, without splitting fields of multiple bytes. The Page Length shall be set in the pages of the MODE SELECT commands to the exact same value (zero value included) returned by the target in the MODE SENSE Page Length bytes. Otherwise, the target shall create CHECK CONDITION status with the Sense Key of ILLEGAL REQUEST.

The initiator shall issue a MODE SENSE command requesting the target to return all Changeable values (see PCF field configuration 0 1 in byte 2 of the MODE SENSE CDB) prior to issuing any MODE SELECT commands, in order to find out which Pages are implemented by the target and the length of each Page.

- Those Pages, supported by the target, in which the initiator requests parameters to be changed shall be sent to the target.
- The initiator may send in MODE SELECT commands all Pages supported by the target.
- The Pages are not required to be sent in ascending order.

In the event of a Hard Reset, the target shall first attempt to restore the Saved Parameters. If Saved Parameters are not available, the target will restore to Default values.

If any bits or bytes in the parameter list are incorrect, the drive will return CHECK CONDITION status with a SENSE KEY of ILLEGAL REQUEST and an ERROR CODE of 26H. The command will not change any pages.

<u>Page Code (H)</u>	<u>Meaning</u>
0	Unit Attention
1	Error Recovery Parameters
2	Disconnect/Reconnect Control Parameters
3	Direct Access Device Format Parameters
4	Rigid Disk Drive Geometry Parameters
6	Certification Pattern
7 through 1F	Reserved
20	Serial Number
21	Date of Manufacture
23	System Flags
24	Manufacturing Control
25	User Page A
26	User Page B
3A through 3B	Reserved
3F	Defined in MODE SENSE only

It is recommended that the initiator issue the RESERVE UNIT command prior to executing the MODE SELECT command, then issue the RELEASE UNIT command after completion of the FORMAT UNIT command. This procedure will prevent any other initiator from issuing different MODE SELECT parameters to the unit prior to execution of the FORMAT UNIT command. The initiator may request that the parameter of Pages 1 and 2 be changed at any time.

The target shall create the CHECK CONDITION Status with Sense Key of UNIT ATTENTION to the first command received from other initiators, when the target has changed Mode Select parameters. The change may be due to a MODE SELECT command issued from a different or from the same initiator.

UNIT ATTENTION PARAMETERS Page Code 0_H

Bit	7	6	5	4	3	2	1	0
Byte								
0	R	R		Page Code = 0 _H				
1				Page Length (in bytes) = 02				
2	0	0	0	Unit Attn	0	0	0	0
3	Reserved							

When bit four (4) of byte two (2) is SET (1), then Unit Attention is logged in sense only; no Check Condition Status will be presented following any *reset*. When this bit is RESET (0) then Check Condition is presented for all effected Initiators following a *reset* until Request Sense is issued by each Initiator (as per current operation).

Page Zero is stored on the drive and is not changed by power off/on cycles or Mode Select commands which do not access page zero. The default state of UnitAttn is Reset.

ERROR RECOVERY PARAMETERS Page Code I_H

Bit	7	6	5	4	3	2	1	0
Byte								
0	R	R	Page Code = 1 _H					
1	Page Length (in bytes) = 06 _H							
2		0		0		0		PER DTE DCR
3	Retry Count							
4	Correction Span							
5	00 _H							
6	00 _H							
7	00 _H							

A **DCR (Disable Correction)** bit 0 set to one indicates that error correction shall not be applied in the course of error recovery. Other normal error recovery operations are not affected by this bit.

A **DCR** bit set to zero enables error correction.

A **DTE (Disable Transfer on Error)** bit 1 set to one and if the **PER** is set to one, indicates that the target shall create the **CHECK CONDITION** status and terminate the data transfer to the initiator immediately upon detection of an error. The Transfer Length is then not exhausted. The data of the block in error, which is first erring block encountered, may or may not be transferred to the initiator depending upon the setting of the **TB** bit. The **DTE** bit can only be set to one by the initiator if the **PER** bit of zero and **DTE** bit set to one.

A **DTE** bit set to zero enables the data transfer for any data which can be recovered within the limits of the Error Recovery Flags. Any erring block that would be posted, which is the last recovered block encountered, is not posted until the Transfer Length is exhausted.

A **PER (Post Error)** bit 2 set to one indicates that the target shall enable the reporting of the **CHECK CONDITION** status for recovered errors, with the appropriate Sense Key. The **CHECK CONDITION** status shall happen during the data transfer depending either on the **DTE** bit value or if an unrecoverable error occurred. If multiple errors occur, the **REQUEST SENSE** data shall report the block address of either the last block on which recovered error occurred or of the first unrecoverable error.

A **PER** bit set to zero indicates that the target shall not create the **CHECK CONDITION** status for errors recovered within the limits established by the other Error Recovery Flags. Recovery procedures exceeding the limits established by the other Error Recovery Flags shall be posted accordingly by the target. The transfer of data may terminate prior to exhausting the Transfer Length depending on the error and the state of the other Error Recovery Flags.

A **TB (Transfer Block)** bit 5 set to one indicates that the failing data block (recovered or unrecoverable) data shall be transferred to the initiator.

A **TB** bit set to zero indicates that the failing data block (recovered or unrecoverable) data shall not be transferred to the initiator.

RETRY COUNT (BYTE 3) is the number of times that the drive will attempt its read algorithm. This is performed before applying correction. This can be set by the initiator to any value from 0 (no retries) to FFH (255 retries).

CORRECTION SPAN (BYTE 4) is the size of the largest read data error, in bits, on which correction may be attempted. This can be set by the initiator to any value from 01H to 0BH.

DISCONNECT/RECONNECT CONTROL PARAMETERS Page Code 2_H

Bit	7	6	5	4	3	2	1	0
Byte								
0	R	R						
1								
2								
3								
4								
5								
6								
7								
8								
9								
10								
11								

Page Code = 2_H

Page Length (in bytes) = 0AH

00H

00H

00H

00H

00H

00H

00H

00H

Reserved

Reserved

This page is accepted, but ignored and reported as all zeros.

DIRECT ACCESS DEVICE FORMAT PARAMETERS Page Code 3_H

Bit	7	6	5	4	3	2	1	0
Byte								

0	R		R		Page Code = 3 _H			
1	Page Length (in bytes) = 16H							

HANDLING OF DEFECTS FIELDS

2*	Tracks per Zone (MSB)
3*	Tracks per Zone (LSB)
4*	Alternate Sectors per Zone (MSB)
5*	Alternate Sectors per Zone (LSB)
6*	Alternate Tracks per Zone (MSB)
7*	Alternate Tracks per Zone (LSB)
8*	Alternate Tracks per volume (MSB)
9*	Alternate Tracks per volume (LSB)

TRACK FORMAT FIELD

10*	00H
11*	Sectors per Track (LSB)

SECTOR FORMAT FIELDS

12	Data Bytes per Physical Sector (MSB)
13	Data Bytes per Physical Sector (LSB)
14*	00H
15*	Interleave (LSB)
16	Track Skew Factor (MSB)
17	Track Skew Factor (LSB)
18	Cylinder Skew Factor (MSB)
19	Cylinder Skew Factor (LSB)

DRIVE TYPE FIELD

Bit	7	6	5	4	3	2	1	0	
20	1		0		0		0		Reserved
21	Reserved								
22	Reserved								
23	Reserved								

Bytes marked (*) are read only (MODE SENSE). They should be set to 00H during a MODE SELECT command.

Any change made to this page by the initiator will not come into effect until a FORMAT UNIT command is issued.

Sectors per track (byte 11) is read only and returns the number of logical sectors per track on the drive.

Bytes per Sector (bytes 12 and 13) can be set by the initiator to any value between 128 and 4096.

Interleave (byte 15) is read only and is a copy of the interleave value used on the last FORMAT UNIT command.

Track Skew Factor (bytes 16 & 17) indicates the number of physical sectors between the last logical block of one track and the first logical block on the next sequential track of the same cylinder.

Cylinder Skew Factor (bytes 18 & 19) indicates the number of physical sectors between the last logical block of one cylinder and the first logical block on the next sequential cylinder.

RIGID DISK DRIVE GEOMETRY PARAMETERS Page Code 4_H

Bit	7	6	5	4	3	2	1	0
Byte								
0	R	R	Page Code = 4 _H					
1	Page Length (in bytes) = 12H							
2*	00H							
3	Number of Cylinders							
4	Number of Cylinders (LSB)							
5	Number of Heads							
6*	00H							
7*	00H							
8*	00H							
9*	00H							
10*	00H							
11*	00H							
12*	00H							
13*	00H							
14*	00H							
15*	00H							
16*	00H							
17	Reserved							
18	Reserved							
19	Reserved							

Bytes marked (*) are read only (MODE SENSE) and should be set to 00H by the initiator.

Any change made to this page by the initiator will not come into effect until a FORMAT UNIT command is issued.

Number of Cylinders (bytes 3 and 4) can be set by the initiator to any value from 0 to 306.

Number of Heads (byte 5) can be set by the initiator to any value from 1 to 4.

CERTIFICATION PATTERN Page Code 6_H

Bit	7	6	5	4	3	2	1	0
Byte								
0	R		R		Page Code = 6 _H			
1	Page Length (in bytes) = 02H							
2	Reserved							
3	Reserved							

This Page is intended to provide the pattern to be used by the target to fill out the data fields of the logical blocks during the FORMAT UNIT command.

SERIAL NUMBER Page Code 20_H

Bit	7	6	5	4	3	2	1	0
Byte								
0	R		R		Page Code = 20 _H			
1	Page Length (in bytes) = 0AH							
2	X							
3	X							
4	X	DRIVE SERIAL NUMBER IN ASCII						
5	X							
6	X							
7	X							
8	X							
9	X							
10				00H				
11				00H				

It is recommended that the initiator does not attempt to modify this page.

DATE OF MANUFACTURE Page Code 21_H

Bit	7	6	5	4	3	2	1	0
Byte								
0	R	R						
1								
2								
3								
4								
5								
6								
7								

Page Code = 21_H

Page Length (in bytes) = 06H

YEAR

WEEK

PLANT CODE | DRIVE TYPE

BUILD LEVEL

BUILD TYPE

BUILD OPTION

It is recommended that the initiator does not attempt to modify this page.

SYSTEM FLAGS Page Code 23_H

Bit	7	6	5	4	3	2	1	0
Byte								
0	R	R	Page Code = 23 _H					
1	Page Length (in bytes) = 02 _H							
2	P	R	R	R	R	R	R	R
3	0	0	0	0	SID		ID	

If P = 1, then parity checking is enabled on the drive.

If P = 0, then parity checking is disabled.

If SID = 1, then the drive uses the software selectable ID in bits 0 to 2.

If SID = 0, then the drive uses the ID defined by the ID selector as shown in Figure 10.3.2.

MANUFACTURING CONTROL Page Code 24_H

Bit	7	6	5	4	3	2	1	0
Byte								
0	R		R		Page Code = 24 _H			
1	Page Length (in bytes) = 02H							
2	COUNTER MSB							
3	COUNTER LSB							

This is a read only page.

This counter is used during manufacturing for process control.

USER PAGE A Page Code 25_H

Bit	7	6	5	4	3	2	1	0
Byte								
0	R		R		Page Code = 25 _H			
1	Page Length (in bytes) = 06H							
2	USER DATA							
3	USER DATA							
4	USER DATA							
5	USER DATA							
6	USER DATA							
7	USER DATA							

This page may be used by the initiator to keep system data.

USER PAGE B Page Code 26_H

Bit	7	6	5	4	3	2	1	0
Byte								
0	R		R		Page Code = 26 _H			
1	Page Length (in bytes) = 06H							
2	USER DATA							
3	USER DATA							
4	USER DATA							
5	USER DATA							
6	USER DATA							
7	USER DATA							

The bytes on this page may be written once only. Any further writes will be ignored.

This page is intended for customer unique identification which is permanently stored on the drive and cannot be changed.

13.11 RESERVE CommandOperation Code: 16_HTABLE 13.11 : RESERVE COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			3rdPty	Third Party Device ID			Extent
2	Reservation Identification							
3	Extent List Length (MSB)							
4	Extent List Length (LSB)							
5	Reserved						Flag	Link

The RESERVE command is used to reserve logical units or, extents within logical units for the use of the initiator. Third-party reservation is implemented. The logical units or extents may be reserved for another specified SCSI device. The RESERVE and RELEASE commands provide the basic mechanism for contention resolution in multiple-initiator systems.

13.11.1 Logical Unit Reservation

If the extent bit is zero, this command shall request that the entire logical unit be reserved for the exclusive use of the initiator until the reservation is superceded by another valid RESERVE command from the initiator that made the reservation or until released by a RELEASE command from the same initiator, by a BUS DEVICE RESET message from any initiator, or by a "hard" RESET condition. A logical unit reservation shall not be granted if the logical unit or any extent is reserved by another initiator. It shall be permissible for an initiator to reserve a logical unit that is currently reserved by that initiator. If the extent bit is zero, the reservation identification and the extent list length shall be ignored.

If the logical unit, or any extent within the logical unit is reserved for another initiator, the target shall respond by returning a RESERVATION CONFLICT status.

If, after honoring the reservation, any other initiator then subsequently attempts to perform any command on the reserved logical unit other than a RELEASE command, which shall be ignored, then the command shall be rejected with RESERVATION CONFLICT status.

13.11.2 Extent Reservation

The reservation identification provides a means for an initiator to identify each extent reservation. This allows an initiator in a multiple tasking environment, to have multiple reservations outstanding. The reservation identification is used in the RELEASE command to specify which reservation is to be released. It is also used in superceding RESERVE commands to specify which reservation is to be superceded.

If the extent bit is one then the target shall process the reservation on request as follows:

- (1) The extent list shall be checked for the number of extents in the reservation request. If the extent list length is zero, no reservations shall be changed and this condition shall not be treated as an error. If the extent list contains more extents than are supported on the logical unit, the command shall be terminated with a CHECK CONDITION status and the sense key shall be set to ILLEGAL REQUEST. If the extent list contains more extents than are currently available on the logical unit, then the target shall return RESERVATION CONFLICT status. The RO 650 supports a maximum of 15 extents.
- (2) The extent list shall be checked for valid extent logical block addresses. If any logical block address is invalid for this logical unit, the command shall be terminated with a CHECK CONDITION status and the sense key shall be set to ILLEGAL REQUEST. The extent list shall be checked for invalid extent overlaps (as defined by reservation type) with other extent descriptors in the extent list and if invalid overlaps are found, the command shall be terminated with a CHECK CONDITION status and the sense key shall be set to ILLEGAL REQUEST.
- (3) If the requested reservation does not conflict with any active or previously requested reservation, the extents specified shall be reserved until superceded by another valid RESERVE command from the initiator that made the reservation or until released by a RELEASE command from the same initiator, by a BUS DEVICE RESET message from any initiator, or by a "hard" RESET condition. If either of the last two conditions occur, the next command from each initiator shall be terminated with a CHECK CONDITION status and the sense key shall be set to UNIT ATTENTION.

- (4) If the reservation request conflicts with a reservation already active then the target shall return RESERVATION CONFLICT status. Reservations are only made active when all extents are free from conflict with active reservations.

TABLE 13.11.2 : DATA FORMAT OF EXTENT DESCRIPTORS

Bit	7	6	5	4	3	2	1	0
Byte								
0	Reserved					0	Reservation Type	
1	Number of Blocks (MSB)							
2	Number of Blocks							
3	Number of Blocks (LSB)							
4	Logical Block Address (MSB)							
5	Logical Block Address							
6	Logical Block Address							
7	Logical Block Address (LSB)							

The size of the extent list shall be defined by the extent list length parameter. The extent list shall consist of zero or more descriptors as shown in Table 13.11.2. Each extent descriptor defines an extent beginning at the specified logical block address for the specified number of blocks. If the number of blocks is zero, the extent shall begin at the specified logical block address and continue through the last logical block address on the logical unit.

The reservation type field shall determine the type of reservation to be effected for each extent. Four types of reservations are possible as follows:

<u>DB(1)</u>	<u>DB(0)</u>	<u>RESERVATION TYPE</u>
1	0	Read Exclusive
0	1	Write Exclusive
1	1	Exclusive Access
0	0	Read Shared

Read Exclusive

While this reservation is active, no other initiator shall be permitted read operations to the indicated extent. This reservation shall not inhibit write operations from any initiator or conflict with a write exclusive reservation; however, read exclusive, exclusive access, and read shared reservations that overlap this extent shall conflict with this reservation.

Write Exclusive

While this reservation is active, no other initiator shall be permitted write operations to the indicated extent. This reservation shall not inhibit read operations from any initiator or conflict with a read exclusive reservation from any initiator. This reservation shall conflict with write exclusive, exclusive access, and read shared reservations that overlap this extent.

Exclusive Access

While this reservation is active, no other initiator shall be permitted any access to the indicated extent. All reservation types that overlap this extent shall conflict with this reservation.

Read Shared

While this reservation is active, no write operations shall be permitted by any initiator to the indicated extent. This reservation shall not inhibit read operations from any initiator or conflict with a read shared reservation. Read exclusive, write exclusive, and exclusive access reservations that overlap with this extent shall conflict with this reservation.

If an initiator attempts a command to a logical block that has been reserved and that access is prohibited by the reservation, the command shall not be performed and the command shall be terminated with a RESERVATION CONFLICT status. If a reservation conflict precludes any part of the command, none of the commands shall be performed. COPY commands shall be terminated with a CHECK CONDITION status and the sense key shall be set to DATA PROTECT if any part of the copy operation is prohibited by an active reservation. If any extent in a logical unit is reserved in any way, a FORMAT UNIT command shall be rejected with a RESERVATION CONFLICT status.

13.11.3 Third Party Reservation

The third-party reservation option for the RESERVE command allows an initiator to reserve a logical unit or extents within a logical unit for another SCSI device. This option is intended for use in multiple-initiator systems that use the COPY command.

If the third-party (3rdPty) bit is zero, then the third-party reservation option is not requested. If the 3rd Pty bit is one then the RESERVE command shall reserve the specified logical unit or extents for the SCSI device specified in the third-party device ID field. The target shall preserve the reservation until it is superseded by another valid RESERVE command from the initiator that made the reservation or until it is released by the same initiator, by a BUS DEVICE RESET message from any initiator, or a "hard" RESET condition. The target shall ignore any attempt to release the reservation made by any other initiator.

13.11.4 Superseding Reservations

An initiator that holds a current reservation may modify that reservation by issuing another RESERVE command to the same logical unit and, if the extent bit is one, using the same reservation identification. The superseding RESERVE command shall release the previous reservation state when the new reservation request is granted. The previous reservation shall not be modified if the new reservation request cannot be granted. If the superseding reservation cannot be granted because of conflicts with a previous active reservation (other than the reservation being superseded), then the target shall return RESERVATION CONFLICT status.

Superseding reservations are principally intended to allow the SCSI device ID to be changed on a reservation using the third-party reservation option. This capability is necessary for certain situations when using the COPY command.

13.12 RELEASE CommandOperation Code: 17_HTABLE 13.12 : RELEASE COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			3rdPty	Third Party Device ID			Extent
2	Reservation Identification							
3	Reserved							
4	Reserved							
5	Reserved						Flag	Link

The RELEASE command is used to release previously reserved logical units, or previously reserved extents within logical units. It is not an error for an initiator to attempt to release a reservation that is not currently active. In this case, the target returns GOOD status without altering any other reservation.

13.12.1 Logical Unit Release

If the extent bit is zero, this command shall cause the target to terminate all logical unit and extent reservations that are active from the initiator to the specified logical unit.

13.12.2 Extent Release

If the extent bit is one this command shall cause any reservation from the requesting initiator with a matching reservation identification to be terminated. Other reservations from the requesting initiator shall remain in effect.

13.12.3 Third Party Release

The third-party release option for the RELEASE command allows an initiator to release a logical unit or extents within a logical unit that were previously reserved using the third-party reservation option. This option is intended for use in multiple-initiator systems that use the COPY command.

If the third-party (3rdPty) bit is zero, then the third-party release option is not required. If the 3rdPty bit is one then the target shall release the specified logical unit or extents, but only if the reservation was made using the third-party reservation option by the initiator that is requesting the release for the same SCSI device as specified in the third-party device ID field.

13.13 MODE SENSE CommandOperation Code: 1A_HTABLE 13.13.1 : MODE SENSE COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	LUN				Reserved			
2	PCF		Page Code					
3	Reserved							
4	Allocation Length							
5	Reserved						Flag	Link

The MODE SENSE command provides a means for a target to report its medium, logical unit, target or peripheral device parameters to the initiator. It is a complementary command to the MODE SELECT command.

The PCF (Page Control Field) bits 7 and 6 of byte 2 defines the type of Page Parameter values to be returned. Either:

- Current
- Changeable
- Default
- or Saved

The Page Code bits 5 through 0 of byte 2 indicates which Page(s) to return.

The Allocation Length specifies the number of bytes that the initiator has allocated for returned MODE SENSE data. An Allocation Length of zero indicates that no MODE SENSE data shall be transferred. This condition shall not be considered as an error. Any other value indicates the maximum number of bytes that shall be transferred. The target shall terminate the DATA IN phase when the Allocation Length have been transferred or when all available MODE SENSE data have been transferred to the initiator, whichever is less.

The MODE SENSE data (Table 13.13.2) contains a four-byte header, followed by zero or more eight-byte block descriptors, followed by zero or more Pages.

Page Code Field bits 7 and 6 byte 2 of the CDB.

7 6

0 0 Report Current Values

- If the Page Code is equal to $3F_H$, all Pages (except Page 0) implemented by the target will be returned to the initiator with fields and bits set to Current values.
- If the Page Code is different than $3F_H$, the Page defined by the Page Code, if supported by the target, will be returned to the initiator with fields and bits set to Current Values.

The Current values are either:

- as set in the last successfully completed MODE SELECT command.
- or are identical to the Saved values and if no MODE SELECT command were yet issued since the last power on.
- or are identical to the Default values if no Saved values are available.

Fields and bits not supported by the target will be set to zero.

The Page Length byte value of each Page returned by the target indicates up to which field are supported within the particular Page.

0 1 Report Changeable Values

- If the Page Code is equal to $3F_H$, all Pages (except Page 0) implemented by the target will be returned to the initiator with bits and fields that are allowed to be changed by the initiator shall be set to zero.
- If the Page Code is different than $3F_H$, the Page defined by the Page Code, if supported by the target, will be returned to the initiator with bits and fields that are allowed to be changed by the initiator shall be set to one. Fields and bits not allowed to be changed by the initiator shall be set to zero.

If no bits or fields are changeable within a Page, the target will return the Page with the Page Length byte value set to zero.

The Page Length byte value of each Page returned by the target indicates up to which field are supported within the particular Page.

1 0 Report Default Values

- If the Page Code is equal to $3F_H$, all Pages (except Page 0) implemented by the target will be returned to the initiator with fields and bits set to the default values.
- If the Page Code is different than $3F_H$, the Page defined by the Page Code, if supported by the target, will be returned to the initiator with fields and bits set to the default values.

Fields and bits not supported by the target will be set to zero.

The Page Length byte value of each Page returned by the target indicates up to which field are supported within the particular Page.

1 1 Report Saved Values

- If the Page Code is equal to $3F_H$, all Pages (except Page 0) implemented by the target will be returned to the initiator with fields and bits set to the saved values.
- If the Page Code is different than $3F_H$, the Page defined by the Page Code, if supported by the target, will be returned to the initiator with fields and bits set to the saved values.

The Saved values are the values saved during the last successfully completed FORMAT UNIT or MODE SELECT commands.

Fields and bits not supported by the target will be set to zero.

The Page Length byte value of each Page returned by the target indicates up to which field are supported within the particular Page.

Current values may be modified by successfully completed MODE SELECT commands. Saved values may only be updated by a successfully completed FORMAT UNIT command. A FORMAT UNIT command completing with No CHECK CONDITION status shall indicate that the Saved values have been successfully saved.

An initiator may request a particular Page to be returned by the target by selecting its code in byte two of the CDB.

<u>PAGE CODE</u>	<u>MEANING</u>
1 _H	Error Recovery parameters
2 _H	Disconnect/Reconnect Control parameters
3 _H	Direct Access Device Format parameters
4 _H	Rigid Disk Drive Geometry parameters
6 _H	Certification Pattern
7 _H through 1F _H	Reserved
20 _H	Drive Serial Number
21 _H	Date of Manufacture
23 _H	System Flags
24 _H	Manufacturing Control
25 _H	User Page A
26 _H	User Page B
3F _H	Return all pages to initiator. See PCF bit configuration. Valid for mode sense commands only.

TABLE 13.13.2 : MODE SENSE DATA MODE SENSE HEADER

Bit	7	6	5	4	3	2	1	0
Byte								
0	Sense Data Length							
1	Medium Type (00)							
2	Reserved							
3	Block Descriptor Length (08)							
Block Descriptor(s)								
0	Density Code (00)							
1	Number of Blocks (MSB) (00)							
2	Number of Blocks (00)							
3	Number of Blocks (LSB) (00)							
4	Reserved							
5	Block Length (MSB)							
6	Block Length							
7	Block Length (LSB)							
Page Descriptor(s)								
0	PS	R	Page Code					
1	Page Length (in bytes)							
2 to n	Refer to Page definition in MODE SELECT							

The Sense Data Length byte specifies the length in bytes of the following MODE SENSE data that is available to be transferred during the DATA IN phase. The Sense Data Length byte shall not include itself. If the Allocation Length of the CDB is too small to transfer all of the Sense Data Length, the Sense Data Length shall not be adjusted to reflect the truncation.

Optional additional blocks of parameters called "Pages" may be sent to the target in the Data Out phase of the MODE SELECT command, following either:

- the MODE SELECT Header, if the Block Descriptor length is set to zero.
- or all Block Descriptors, if the Block Descriptor length is set to zero.

The Block Descriptor Length shall not include the length of the Pages.

Each defined Page is preceded by a Header of two bytes defining the Page Code and the length of the page. Following the Header the Pages are separated into sub-blocks containing a list of related flags and/or values.

PS (Parameters Saveable) bit 7 byte 0 of each Page Header set to one by the target indicates that the supported parameters can be saved by the target. PS set to zero indicates that the supported parameters cannot be saved by the target.

Bits 6 of byte 0 is reserved.

The Page Code identifies the meaning of the following bytes in the Page.

The Page Length indicates the number of bytes that the target supports in each Page. The Page Length value of each defined page, shall not include the Page Length byte. The target will return in the Pages of the MODE SENSE commands as many consecutive bytes that it supports, for each Page that it supports, without splitting fields of multiple bytes. The Page Length shall be set in the pages of the MODE SELECT commands to the exact same value (zero value included) returned by the target in the MODE SENSE Page Length bytes. Otherwise, the target shall create CHECK CONDITION status with the Sense Key of ILLEGAL REQUEST.

The initiator shall issue a MODE SENSE command requesting the target to return all Changeable values (PCF field configuration 0 1 and Page Code 3F_H in byte 2 of the MODE SENSE CDB) prior to issuing any MODE SELECT commands, in order to find out which Pages are implemented by the target and the length of each Page.

13.14 START/STOP UNIT CommandOperation Code: 1B_HTABLE 13.14 : START/STOP UNIT COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved				Immed
2	Reserved							
3	Reserved							
4	Reserved							Start
5	Reserved						Flag	Link

The START/STOP UNIT command requests that the target enable or disable the unit for further operations.

An immediate (Immed) bit of one indicates that status shall be returned as soon as the operation is initiated. An Immed bit of zero indicates that status shall be returned after the operation is completed.

A start bit of one requests the unit be made ready for use. A start bit of zero requests that the unit be stopped.

When the unit is stopped, the head positioner is parked at cylinder 305 and power is removed from the spindle and stepper motors.

13.15 SEND DIAGNOSTIC CommandOperation Code: 1D_HTABLE 13.15 : SEND DIAGNOSTIC COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved		1	0	0
2	Reserved							
3	00H							
4	00H							
5	Reserved						Flag	Link

The following tests are done:

- ROM CHECK adds all the ROM bytes and checks for zero. Will return CHECK CONDITION status with a ROM DIAGNOSTIC FAILURE sense code.
- RAM CHECK checks the buffer RAM with a walking one pattern. Will return CHECK CONDITION status with a HARDWARE ERROR sense key and RAM DIAGNOSTIC FAILURE sense code.
- READ/WRITE TEST writes a pattern to a special sector on the maintenance track, reads back and does a byte comparison. Repeated for 256 different patterns. Will return CHECK CONDITION status with a HARDWARE ERROR sense key.

None of the above tests will destroy the user's data.

13.16 READ CAPACITY CommandOperation Code: 25_HTABLE 13.16.1 : READ CAPACITY COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved				0
2	Logical Block Address (MSB)							
3	Logical Block Address							
4	Logical Block Address							
5	Logical Block Address (LSB)							
6	Reserved							
7	Reserved							
8	Reserved							PMI
9	Reserved						Flag	Link

The READ CAPACITY command provides a means for the initiator to request information regarding the capacity of the logical unit.

A partial medium indicator (PMI) bit of zero indicates that the information returned in the READ CAPACITY data shall be the logical block address and block length (in bytes) of the last logical block of the logical unit. The logical block address in the command descriptor block shall be set to zero for this option.

A PMI bit of one indicates that the information returned shall be the logical block address and block length (in bytes) of the last logical block address after which a substantial delay in data transfer will be encountered. This logical block address shall be greater than or equal to the logical block address specified in the command descriptor block.

The eight bytes of READ CAPACITY data shown in Table 13.16.2 shall be sent during the DATA IN phase of the command.

TABLE 13.16.2 : READ CAPACITY DATA

BYTE	DESCRIPTION
0	Logical Block Address (MSB)
1	Logical Block Address
2	Logical Block Address
3	Logical Block Address (LSB)
4	Block Length (MSB)
5	Block Length
6	Block Length
7	Block Length (LSB)

13.17 READ Command (Extended)Operation Code: 28_HTABLE 13.17 : READ COMMAND (EXTENDED)

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved				0
2	Logical Block Address (MSB)							
3	Logical Block Address							
4	Logical Block Address							
5	Logical Block Address (LSB)							
6	Reserved							
7	Transfer Length (MSB)							
8	Transfer Length (LSB)							
9	Reserved					Flag		Link

The READ EXTENDED command is identical to the READ command except a two byte transfer length is available.

13.18 WRITE Command (Extended)Operation Code: 2A_HTABLE 13.18 : WRITE COMMAND (EXTENDED)

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved				1
2	Logical Block Address (MSB)							
3	Logical Block Address							
4	Logical Block Address							
5	Logical Block Address (LSB)							
6	Reserved							
7	Transfer Length (MSB)							
8	Transfer Length (LSB)							
9	Reserved					Flag		Link

The WRITE EXTENDED command is identical to the WRITE command except a two byte transfer length is available.

13.19 VERIFY CommandOperation Code: 2F_HTABLE 13.19 : VERIFY COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved			0	0
2	Logical Block Address (MSB)							
3	Logical Block Address							
4	Logical Block Address							
5	Logical Block Address (LSB)							
6	Reserved							
7	Verification Length (MSB)							
8	Verification Length (LSB)							
9	Reserved						Flag	Link

The command is identical to the READ command except that the read data is not transferred across the interface. The status phase will occur immediately after the command phase.

A verification length of zero indicates that no logical blocks will be verified.

The header and data fields will be checked for CRC and ECC errors respectively; the status byte indicating if an error was detected.

13.20 READ DEFECT DATA CommandOperation Code: 37_HTABLE 13.20 : READ DEFECT DATA COMMAND

Bit	7	6	5	4	3	2	1	0
Byte								
0	Operation Code							
1	Logical Unit Number			Reserved				
2	0	0	0	P	G	Code		
3	Reserved							
4	Reserved							
5	Reserved							
6	Reserved							
7	Allocation Length (MSB)							
8	Allocation Length							
9	Reserved					Flag	Link	

The READ DEFECT DATA command requests the drive to transfer the medium defect data to the initiator.

The CODE field of Byte 2 refers to a three bit code which defines the required format of the defect list. Only two codes are supported:

- 100 Bytes from index format (PLIST ONLY)
- 101 Physical sector format

Any other code will cause a Check Condition status with an Illegal Request Sense Key.

The initiator indicates with this field a preferred format for the defect list to be returned by the drive.

The P bit set to one indicates that the initiator requests that the Primary list of defects be returned. The P bit of zero indicates that the drive will not return the Primary list of defects.

The G bit set to one indicates that the initiator request that the Growing list of defects be returned. The G bit of zero indicates that the drive will not return the Growing list of defects.

With P and G both set to zero, the Defect List Header is only to be returned.

With P and G both set to one, the drive will return the PLIST and the GLIST.

NOTE: If CODE field = 100 (Bytes from index format) the G bit must be 0.

The Allocation Length specifies the number of bytes that the initiator has allocated for returned READ DEFECT DATA. An Allocation Length of zero indicates that no READ DEFECT DATA shall be transferred. Any other value indicates the maximum number of bytes that shall be transferred.

The drive will terminate that DATA IN phase when the Allocation Length have been transferred to the initiator, whichever is less.

The drive could return a maximum of 484 bytes.

The READ DEFECT DATA contains a four byte header, followed by zero or more descriptors.

Defect List Header

Bit		7		6		5		4		3		2		1		0
Byte 0		0		0		0		0		0		0		0		0
Byte 1		0		0		0		P		G		CODE				
Byte 2		DEFECT LIST LENGTH MSB														
Byte 3		DEFECT LIST LENGTH LSB														

The meanings of bits 0 through 2 of Byte 1 are the same as bits 0 through 2 of Byte 2 of the CDB. The bits P, G and the Defect List Format indicates which defect list is actually returned by the target.

The format of the defect descriptors, if the Defect list length is different from zero, are shown below. The length of each defect descriptor is eight bytes. The defect list length specifies the total length in bytes of the defect descriptors that follow. The Defect List Length is equal to eight times the number of defect descriptors. If the Allocation Length of the CDB is too small to transfer all of the defect descriptors, the Defect List Length will not be adjusted to reflect the truncation.

The defect descriptors may not be in ascending order.

The initiator may be informed about the exact number of defects by dividing the Defect List Length by the Defect Descriptor Length.

Defect List Formats

Bytes from Index Format (Code 100)

Byte 0	00H
Byte 1	Cylinder Number MSB
Byte 2	Cylinder Number LSB
Byte 3	Head Number
Byte 4	00H
Byte 5	00H
Byte 6	Bytes from Index MSB
Byte 7	Bytes from Index LSB

Physical Sector Format (Code 101)

Byte 0	00H
Byte 1	Cylinder Number MSB
Byte 2	Cylinder Number LSB
Byte 3	Head Number
Byte 4	00H
Byte 5	00H
Byte 6	00H
Byte 7	Physical Sector Number

13.21 WRITE BUFFER CommandOperation Code: 3B_HTABLE 13.21 : WRITE BUFFER COMMAND

Bit	7	6	5	4	3	2	1	0
Byte 0	OPERATION CODE							
Byte 1	LOGICAL UNIT NUMBER			RESERVED				
Byte 2	00H							
Byte 3	00H							
Byte 4	00H							
Byte 5	00H							
Byte 6	RESERVED							
Byte 7	BYTE TRANSFER LENGTH MSB							
Byte 8	BYTE TRANSFER LENGTH LSB							
Byte 9	RESERVED						FLAG	LINK

The WRITE BUFFER Command is used in conjunction with the READ BUFFER Command as a diagnostic function for testing the drive's data buffer memory and the SCSI bus integrity. There will be no access to the medium during the execution of this command.

The Byte Transfer Length specifies the maximum number of bytes to be transferred to and retained in the drive's data buffer. The Byte Transfer Length contains a four byte header, followed by the WRITE BUFFER data. A Byte Transfer Length of zero indicates that no Write Data Buffer Header and no WRITE BUFFER data will be transferred. This condition will not create the Check Condition status. Up to 4100 bytes of data may be transferred including four bytes of header and up to 4096 bytes of WRITE BUFFER data.

If the Byte Transfer Length is greater than the Available Length plus four reported by the READ BUFFER command, the drive will create the Check Condition status with the Sense Key of ILLEGAL REQUEST and with overflow error code. In this case no data will be transferred from the initiator.

WRITE BUFFER HEADER

Bit		7		6		5		4		3		2		1		0	
Byte 0		RESERVED															
Byte 1		RESERVED															
Byte 2		RESERVED															
Byte 3		RESERVED															

13.22 READ BUFFER CommandOperation Code: 3C_HTABLE 13.22 : READ BUFFER COMMAND

Bit	7	6	5	4	3	2	1	0	
Byte 0	OPERATION CODE								
Byte 1	LOGICAL UNIT NUMBER			RESERVED					
Byte 2				00H					
Byte 3				00H					
Byte 4				00H					
Byte 5				00H					
Byte 6				RESERVED					
Byte 7				ALLOCATION TRANSFER LENGTH MSB					
Byte 8				ALLOCATION TRANSFER LENGTH LSB					
Byte 9				RESERVED				FLAG	LINK

The READ BUFFER Command is used in conjunction with the WRITE BUFFER Command as a diagnostic function for testing the drive's data buffer memory and the SCSI bus integrity. There will be no access to the medium during the execution of this command.

The Allocation Length specifies the maximum number of bytes that the initiator has allocated for returned data. The Allocation Length contains a four byte header, followed by the READ BUFFER data. An Allocation Length of zero indicates that no Read Data Buffer Header and no READ BUFFER data will be transferred. This condition will not create the Check Condition status. This data is to be used by the initiator for comparison with the data pattern sent during the WRITE BUFFER command. Up to 4100 bytes of data may be requested to be transferred including four bytes of header and up to 4096 bytes of READ BUFFER data.

If the Allocation Length is greater than the Available Length plus four, the Available Length and the Read Buffer Header will be transferred to the initiator.

It will not be considered an error to request an Allocation Length less than the Available Length.

The drive will terminate the DATA IN phase when the Allocation Length has been transferred or when the Available Length has been transferred to the initiator, whichever is less.

READ BUFFER HEADER

Bit	7	6	5	4	3	2	1	0
Byte 0	RESERVED							
Byte 1	RESERVED							
Byte 2	AVAILABLE LENGTH MSB							
Byte 3	AVAILABLE LENGTH LSB							

13.23 MAINTENANCE SEEK CommandOperation Code: EO_HTABLE 13.23 : MAINTENANCE SEEK COMMAND

Bit	7	6	5	4	3	2	1	0
Byte 0	OPERATION CODE							
Byte 1	LOGICAL UNIT NUMBER			0	0	0	0	0
Byte 2	CYLINDER NUMBER MSB							
Byte 3	CYLINDER NUMBER MSB							
Byte 4	HEAD NUMBER							
Byte 5	0	0	0	0	0	0	FLAG	LINK

This command enables the initiator to seek to any cylinder and head without using a logical address.

NOTE:

For this command cylinder 0, head 0 is the maintenance track. Cylinder 2, head 0 is the first track normally seen by the user and is equivalent to logical address 0.

13.24 FORMAT MAINTENANCE TRACKS CommandOperation Code: E1_HTABLE 13.24 : FORMAT MAINTENANCE TRACKS COMMAND

Bit		7		6		5		4		3		2		1		0	
Byte 0		OPERATION CODE															
Byte 1		LOGICAL UNIT NUMBER					0		0		0		0		P		
Byte 2		0		1		0		1		0		0		1		0	
Byte 3		0		1		0		0		1		1		1		1	
Byte 4		0		0		0		0		0		0		0		0	
Byte 5		0		0		0		0		0		0		FLAG		LINK	

This command allows the initiator to initialise the maintenance tracks. It also clears the defect list table and resets the mode select parameters to defaults. After this command has been issued, tracks -2 and -1 will have been formatted in the maintenance track format (256 byte sectors x 61). At this time, logical sector 0 is the first sector of the maintenance track. Any read or write command can now access the maintenance tracks. This mode is reset after the first FORMAT UNIT command.

If P = 1 (Byte 1, bit 0) then the PLIST and MODE SELECT parameters will be preserved.

If P = 0 then the PLIST will be deleted and the MODE SELECT parameters will return to default values.

13.25 CERTIFY CommandOperation Code: E2_H

This command can be used to certify and re-assign bad blocks from the media.

TABLE 13.25 : CERTIFY COMMAND

Bit	7	6	5	4	3	2	1	0
Byte 0	OPERATION CODE							
Byte 1	LOGICAL UNIT NUMBER			0	0	0	0	0
Byte 2	0	0	0	0	0	0	0	0
Byte 3	PASS COUNT							
Byte 4	0	0	0	0	0	0	0	0
Byte 5	0	0	0	0	0	0	FLAG	LINK

This command has two distinct modes of operation:

Mode 1 : Drive Formatted in User Format

The entire drive is scanned for defects. The scan is READ ONLY, user data is preserved. The pass count is used to determine the number of read scans. A pass count of 0 will perform one scan. Any errors found will be automatically re-assigned and entered into the GLIST.

Mode 2 : Drive Formatted in All Sector Format (Format Control CODE 1EH)

The certify command performs a Read/Write test and enters any defects into the PLIST. One pass of the Read/Write test is as follows:

- 1 Read Disk
- 2 Write Disk with data 23H
- 3 Read Disk
- 4 Write Disk with data 49H
- 5 Read Disk
- 6 Write Disk with data 6CH
- 7 Read Disk
- 8 Write Disk with data 12H
- 9 Read Disk
- 10 Write Disk with data 49H
- 11 Read Disk

Each pass takes approximately 11 minutes. The sequence may be repeated up to 255 times using the pass count. A new PLIST will be created at the end of the command.

13.26 FAST READ CommandOperation Code: E8_H

This command is the same as READ except no data is transferred to the host. It can be used as a verify command.

TABLE 13.26 : FAST READ COMMAND

Bit	7	6	5	4	3	2	1	0
Byte 0	OPERATION CODE							
Byte 1	LOGICAL UNIT NUMBER			LOGICAL BLOCK ADDRESS (MSB)				
Byte 2	LOGICAL BLOCK ADDRESS							
Byte 3	LOGICAL BLOCK ADDRESS (LSB)							
Byte 4	BLOCK COUNT							
Byte 5	0	0	0	0	0	0	FLAG	LINK

13.27 FAST WRITE CommandOperation Code: EA_H

This command is the same as WRITE except no data is transferred from the host. The sector buffer should be filled with the required data pattern using the WRITE SECTOR BUFFER command.

TABLE 13.27 : FAST WRITE COMMAND

Bit	7	6	5	4	3	2	1	0
Byte 0	OPERATION CODE							
Byte 1	LOGICAL BLOCK ADDRESS			LOGICAL BLOCK ADDRESS (MSB)				
Byte 2	LOGICAL BLOCK ADDRESS							
Byte 3	LOGICAL BLOCK ADDRESS (LSB)							
Byte 4	BLOCK COUNT							
Byte 5	0	0	0	0	0	0	FLAG	LINK

13.28 READ RESERVATIONS Command

Operation Code: EB

TABLE 13.28 : READ RESERVATIONS COMMAND

Bit	7	6	5	4	3	2	1	0
Byte 0	OPERATION CODE							
Byte 1	LOGICAL UNIT NUMBER			0	0	0	0	0
Byte 2	00							
Byte 3	00							
Byte 4	00							
Byte 5							FLAG	LINK

This command returns the drives reservation list during a data phase, in the following format.

HEADER

Bit	7	6	5	4	3	2	1	0
Byte 0	# of EXTENTS				# of RESERVATIONS			
Byte 1	TABLE LENGTH							

RESERVATION HEADER

Bit		7		6		5		4		3		2		1		0
Byte 0		Initiator ID				3rd Party		3rd Party ID				Extents				
Byte 1		Reservation ID														
Byte 2		# of extents in this reservation														

Each extent within the reservation then has 8 bytes with the following format.

Bit		7		6		5		4		3		2		1		0	
Byte 0		Reservation Type															
Byte 1		Length MSB															
Byte 2		Length															
Byte 3		Length															
Byte 4		Length LSB															
Byte 5		Start Block MSB															
Byte 6		Start Block															
Byte 7		Start Block LSB															

13.29 REGISTER TEST Command

Operation Code: EF

TABLE 13.29 : REGISTER TEST COMMAND

Bit	7	6	5	4	3	2	1	0
Byte 0	OPERATION CODE							
Byte 1	LOGICAL UNIT NUMBER			RAM	REG	MEM	UP	R/W
Byte 2	MSB ADDRESS							
Byte 3	LSB ADDRESS							
Byte 4	DATA							
Byte 5	0	0	0	0	0	0	FLAG	LINK

This command allows the initiator to read or write registers or memory locations within the RO 650. The use of this instruction implies an in-depth knowledge of the firmware/hardware structure of the drive.

RAM

If this bit is set the command allows access to internal 8031 RAM locations.

RES

If this bit is set the command allows access to hardware registers within the DMA controller and disc controller chips.

MEM

If this bit is set the command allows access to locations within the sector buffer memory.

UP

If this bit is set together with the MEM bit the upper 4K of the sector buffer will be addressed. If this bit is clear together with the MEM bit set the lower 4K of the sector buffer will be addressed.

R/W

If this bit is set a WRITE will be performed to the selected location using byte 4 as the write data.

BYTES 2 and 3

Bytes 2 and 3 are used to define the required address of the memory location or register.

This command will firstly write to the specified address if the R/W bit is set using the data specified in byte 4 of the CDB. A read is then performed on the specified address and the data read is compared with byte 4 of the CDB. If the read data does not compare with byte 4 of the CDB a CHECK CONDITION STATUS will be returned. A subsequent REQUEST SENSE COMMAND will return the "good" data in byte 6 and the "bad" data in byte 4 of the sense data.

This command may also be used to clear the "BADFORMAT" flag for diagnostic purposes. To do this, bytes 1 to 5 of the CDB should all be set to zero.

14.0 **DEFECT HANDLING**

Disc defects are handled by the RO 650 using a sector sparing technique. During manufacture the drive is formatted using a format control code of 1EH. After this format, the drive allows the initiator access to all physical sectors. The drive is tested in this mode and any defective sectors are entered into a list known as the Primary Defect List or PLIST. The PLIST is stored in sectors 0 and 10 of the special Maintenance Track. This track is physically Cylinder -2, Head 0 and is NOT part of the logical address space normally available to the user. The PLIST can only be altered or erased by reformatting the maintenance track (Command E1H) or reformatting the entire drive (Command 04H) using format control codes 1EH or 16H.

The PLIST is stored in bytes from index format although it may be displayed by the READ DEFECT DATA command in either bytes from index format or physical sector format.

When the drive is formatted using the FORMAT UNIT command with format control codes 00H, 10H or 18H (User Format), the PLIST is searched and any defective sectors are assigned to spares. One sector per track is reserved for sector sparing. Only one defective sector per track is allowed during manufacture. Since the PLIST is stored in bytes from index format the RO 650 can calculate the physical defective sector for any sector size and any interleave factor. Before each track is formatted, the defect list is searched, if there is a defect, the physical sector is calculated and marked as bad. An algorithm then calculates the optimum sector layout to skip any bad sectors and conform to the user defined interleave factor. The track is then formatted and the process repeated until the entire drive is formatted. The drive is shipped with all known defects assigned to spares.

Any additional defects found during the life of the drive may be mapped out using the RE-ASSIGN BLOCKS command. This command used one of two mechanisms to re-assign a defective block:

14.1 If the spare sector is not already used on the track the spare is assigned to the defective sector. This is done as follows:

- 14.1.1 Attempt to read the defective sector with up to 10 retries.
- 14.1.2 Save the data in the sector buffer.
- 14.1.3 Overwrite the header of the defective sector.
- 14.1.4 Modify the header of the spare sector.
- 14.1.5 Re-write the data into the spare.

The data read from the re-assigned sector may be corrupted.

- 14.2 If the spare sector is used, or if 14.1 above fails, the whole track will be re-assigned to one of seven available spare tracks.

This is done as follows:

- 14.2.1 Select the next free spare track.
- 14.2.2 Copy data from the defective track to the spare.
- 14.2.3 Re-format the defective track to point to the spare.

The data read from the re-assigned sector and any other bad sector on the track may be corrupted.

Should the same logical block or any other on that track be subsequently re-assigned by another RE-ASSIGN BLOCK command, the data will be copied from that spare track to the next free spare track and the original defective track will be reformatted to point to the new spare track. This process can continue until all seven spare tracks are used. A track will only be re-assigned once per RE-ASSIGN BLOCK command.

Defects given to the drive during a RE-ASSIGN BLOCK command are appended to a Growing Defect List or GLIST. The GLIST is stored in sectors 3 and 13 of the maintenance track. The GLIST is stored in physical sector format and may be displayed by the READ DEFECT DATA command ONLY in physical sector format. The GLIST may be used, together with the PLIST, during the FORMAT UNIT command with control code 00H or 10H. In this case, the two lists are searched together. On tracks with a single defect, the defect is skipped, on tracks with multiple defects, the track is re-assigned to the next available spare.

The GLIST will be deleted if:

- 14.3 The FORMAT MAINTENANCE TRACKS command is issued.
or;
A FORMAT UNIT command with control code 018H is issued.
or;
The sector size is changed and the drive is reformatted using a FORMAT UNIT command.

TABLE 14.4 : DEFECT HANDLING SPECIFICATION

	CYLINDER	HEAD	FORMAT
MAINTENANCE TRACK	-2	0	256 BYTE SECTOR
SPARE TRACK 1	-2	1	USER FORMAT
SPARE TRACK 2	-2	2	USER FORMAT
SPARE TRACK 3	-2	3	USER FORMAT
SPARE TRACK 4	-1	0	USER FORMAT
SPARE TRACK 5	-1	1	USER FORMAT
SPARE TRACK 6	-1	2	USER FORMAT
SPARE TRACK 7	-1	3	USER FORMAT

PLIST

Maximum number of defective sectors = 30.

GLIST

Maximum number of defective sectors = 30.

Maximum number defective tracks = 7. (Greater than 1 flaw)

15.0 LED ERROR CODES

<u>HEX CODE</u>	<u>DEFINITION</u>
01	The drive has detected that the spindle motor speed is out of tolerance ($\pm 10\%$).
02	Program Memory Checksum Error: during its internal diagnostic, the drive detected a program memory checksum error.
05	RAM error: the drive detected a data error during the RAM sector buffer diagnostic.
06	After stepping the maximum number of cylinders, the drive could not achieve correct track zero status.
07	The spindle motor did not start at power up.
08	Spindle motor failed initial $\pm 1\%$ speed check at power up.

All the above error codes are designated FATAL, and resetting of the drive can only be accomplished by powering off, then on again.

If the drive has a FATAL error, it will switch off power to both the stepper and spindle motors and flash the fatal error code on the SELECT LED on the front panel. The drive will still respond to commands sent across the SCSI interface, but will not execute any of them except TEST DRIVE READY, INQUIRY or REQUEST SENSE.